

SFF-8639 Gen-4 Test Adapter

User Manual



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Introduction

This user's manual documents the SFF-8639 Gen-4 Plug and Receptacle Test Adapters (8639G4-TPA-P and 8639G4-TPA-R). The two test adapter types, shown in Figures 1 and 2, test 8639 interface cables, hosts and devices against the SFF-8639 Gen-4 Specification.

NOTE: The test adapters referred to and illustrated in the "General" section of this User's Manual, reflect the "Universal" SFF-8639 PCIe Gen-4 Test Adapters. Previously, Wilder offered SFF-8639 Test Adapters for specific configurations, MultiLink, SATA and SAS. For PCIe Gen-4 we've consolidated the functionality of these fixtures into one "Universal" SFF-8639 PCIe Gen-4 Test Adapter. Customer's using the SFF-8639 PCIe Gen-4 Test Adapters for specific configurations can now find the associated reference information in Addendum "A" of this document.

The TPA-P and TPA-R test adapter assemblies allow easy access, via SMA connections, to measure or inject data signals. The Receptacle test adapter also provides access to +5V, +12V, and their respective GNDs, via a 4-position Molex power connector. Additionally, the user can access +3.3V, its respective GND, Resets, Wake, Activity, Dual Link Enable, SM Clock, SM Data, and others via an alternate 16-position connector. A mating 16-position connector housing and contacts are provided to connect these 16 signals to a wiring assembly provided by the user.

NOTE: To avoid damaging the cables, use the handling techniques described in the Care and Handling section before making any connections or configuring a test setup.

Always use a static-safe workstation when performing tests, as explained in the "Electrostatic Discharge Information" section.

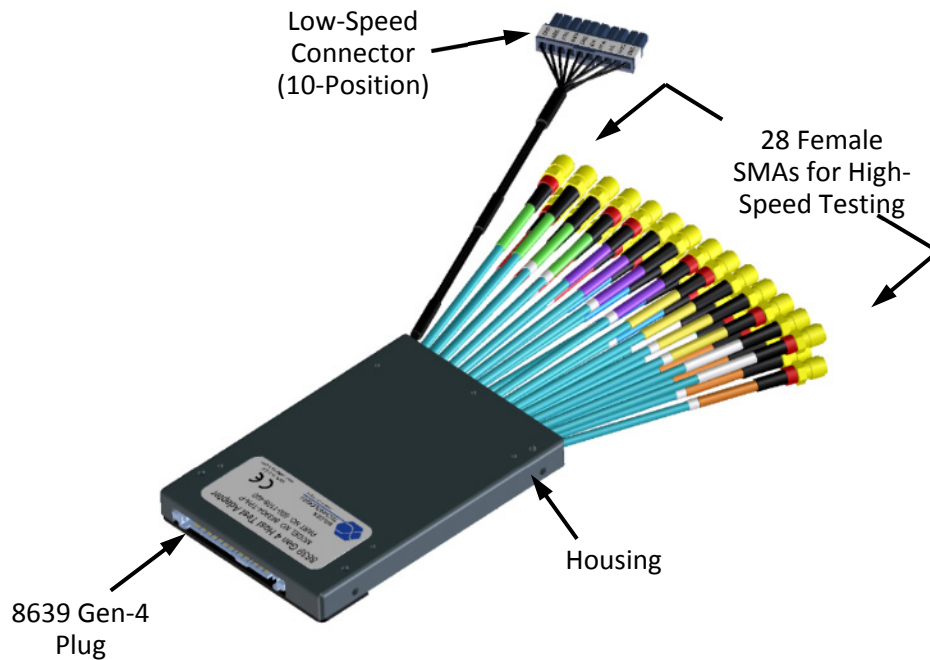


Figure 1. The 8639 Gen-4 Test Adapter (Host Plug). Universal SFF-8639 Gen-4 Host Test Fixture Shown.

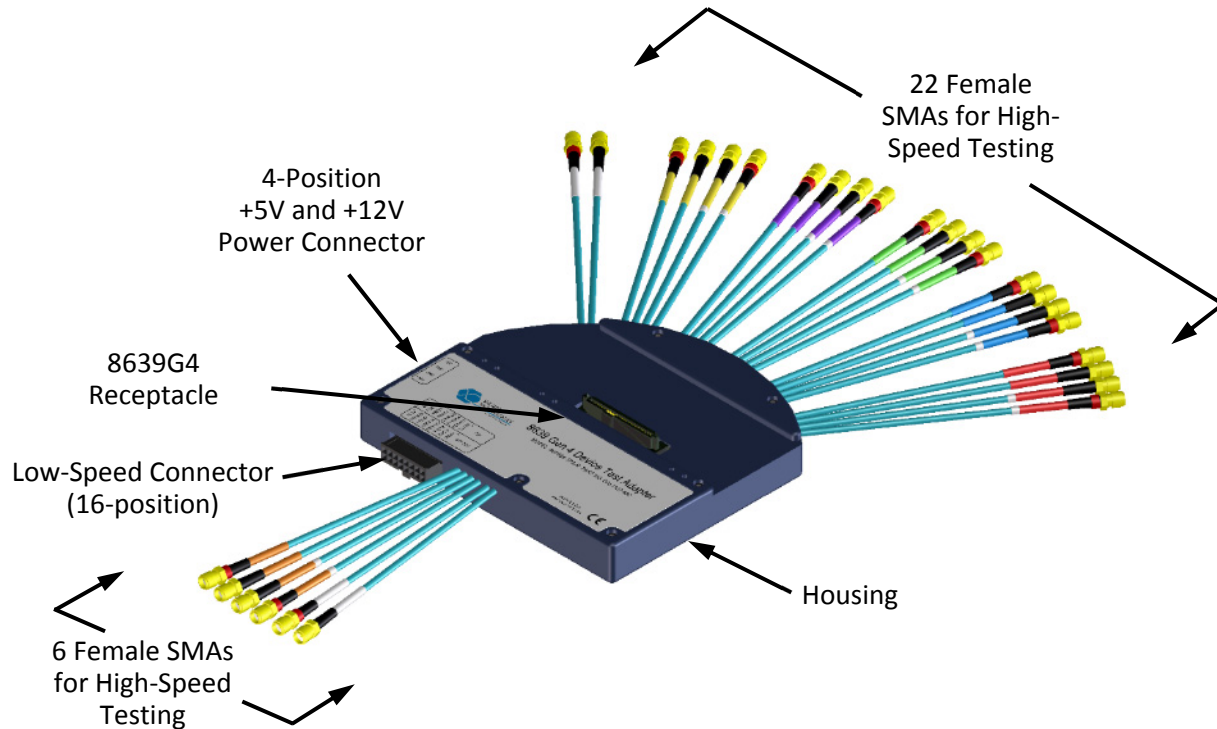


Figure 2. The 8639 Gen-4 Test Adapter (Device Receptacle). Universal SFF-8639 Gen-4 Device Test Fixture Shown. .

The 4-position power connector is Molex part number 53109-0410 (Mating connector not provided). The 16-position keyed/latching mating connector part number is 43045-1602. The mating receptacle connector housing and contact pins for 26-30awg wire are provided with each 8639G4-TPA-R assembly (Molex part numbers 43025-1600 for the 16-position receptacle housing and 43030-0011 for the 26-30awg receptacle contacts). Replacement receptacle parts can be purchased through Molex distributors.

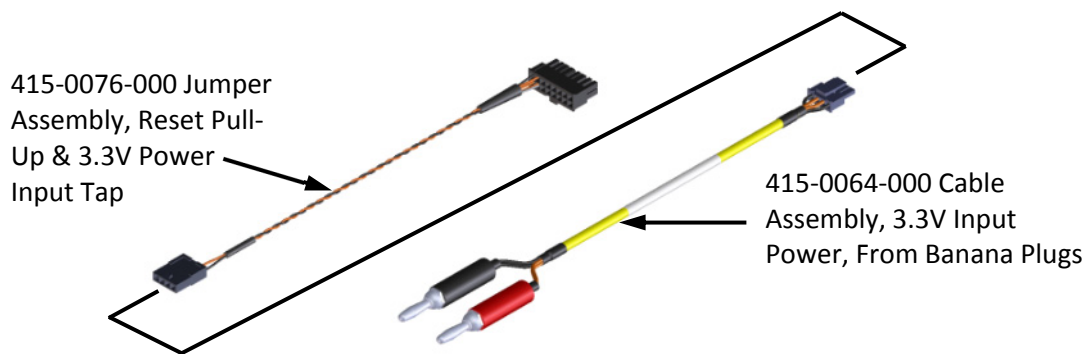


Figure 3. 8639G4-TPA-R Universal TPA Power Cable and Jumper Cable Assemblies

The jumper harness assembly (415-0076-000) and the power in-put cable assembly (415-0064-000) can be used in conjunction to supply 3.3 volts to the TPA and pull-up requirements to PERST and PERSTB. These harness assemblies are provided with the universal receptacle TPA (8639G4-TPA-R).

Product Inspection

Upon receiving the 8639G4-TPA from Wilder Technologies, perform the following product inspection:

- Inspect the outer shipping container, foam-lined instrument case, and product for damage. Retain the outer cardboard shipping container until the contents of the shipment have been inspected for completeness and the product has been checked mechanically and electrically. Use the foam-lined instrument-case for secure storage of the Wilder Technologies SFF-8639 Gen-4 Test Adapter when not in use.
- Locate the shipping list and verify that all items ordered were received.
- In the unlikely event that the product is defective or incomplete, the “Limited Warranty” section discusses how to contact Wilder Technologies for technical assistance and/or how to package the product for return.

The SFF-8639 Gen-4 Test Adapter Care and Handling Precautions

The SFF-8639 Gen-4 Test Adapter requires careful handling to avoid damage. Improper handling techniques, or using too small a cable bend radius, can damage the coaxial cable connections within the adapter housing or the cables themselves. This can occur at any point along the cable. To achieve optimum performance and to prolong the 8639G4-TPA's life, observe the following handling precautions:

- **CAUTION 1: Avoid Torque Forces (Twisting)**
While individual coaxial cables within the test adapter have some rotational freedom, twisting the 8639G4-TPA as a unit, with one end held stationary, may damage or severely degrade performance. Adherence to Caution 5 (below) helps to avoid twisting.
- **CAUTION 2: Avoid Sharp Cable Bends**
Never bend coaxial cables into a radius of 26 mm (1-inch) or less. Never bend cables greater than 90°. Single or multiple cable bends must be kept within this limit. Bending the 8639G4-TPA cables less than a 26mm (1-Inch) radius will permanently damage or severely degrade test adapter performance.
- **CAUTION 3: Avoid Cable Tension (Pull Forces)**
Never apply tension (pull forces) to an individual coaxial cable that is greater than 2.3 kg (5 lbs.). To avoid applying tension, always place accessories and equipment on a surface that allows adjustment to eliminate tension on the 8639G4-TPA and cables. Use adjustable elevation stands or apparatus to accurately place and support the 8639G4-TPA.
- **CAUTION 4: Connect the 8639G4-TPA First**
To prevent twisting, bending, or applying tension to the coaxial cables when connecting a 8639G4-TPA, always attach the 8639G4-TPA to the device under test (DUT) or cable under test before attaching any SMA connectors. Carefully align the 8639G4 connectors and then gently push the connectors together until fully seated.

If the 8639G4-TPA must be turned or twisted to make connection to the DUT, avoid using the 8639G4-TPA housing alone to make this occur. Try to distribute the torque forces along the length of the test setup and cabling. If this is not possible, it is recommended to first loosen or disconnect the SMA connections at the 8639G4-TPA, make the connection to the DUT and then re-tighten or attach the test equipment leads.

NOTE: Only grip the test adapter housing when inserting or extracting the 8639G4-TPA to or from the DUT. Pulling directly on the 8639G4-TPA cables or using them to insert the 8639G4-TPA may cause damage.

- **CAUTION 5: Carefully Make SMA Connections**

To connect the 8639G4-TPA SMA connectors, follow these steps:

1. Hold the cable stationary by grasping the cable at the black heat-shrink section near the SMA connector.
2. Insert the mating SMA barrel and hand-tighten the free-spinning SMA nut onto the connector while avoiding pulling, bending, or twisting the 8639G4-TPA coaxial cable.
3. The 8639G4-TPA SMA connectors have flats that accept an open-end 1/4-inch or 6.5mm wrench. When attaching instrument cables to the 8639G4-TPA, it is recommended that the 8639G4-TPA SMA connectors be mechanically held and the test leads be tightened to the equipment manufacturer's torque recommendations, normally 5 in-lbs, using a 5/16-inch open-end wrench.

If the test set-up requires repositioning, first loosen or disconnect the SMA connections to avoid twisting, bending, or tension.

NOTE: A drop in signal amplitude by half or 6dB during the testing of a channel may indicate that a cable has been mechanically pulled free of coaxial cable connections internal to the assembly. This could be determined by checking if the cable has any lateral play relative to the TPA. This would only occur when the TPA has exceeded the pull force as specified within the mechanical specification. If the cable cannot be re-seated, the test adapter will need to be sent back to the factory for service.

- **CAUTION 6: Independently Support Instrument Cables or Accessories**

Excessive weight from instrument cables and/or accessories connected to the 8639G4-TPA can cause damage or affect the test adapter performance. Be sure to provide appropriate means to support and stabilize all test set-up components.

NOTE: The 8639G4-TPA-R (Device TPA) is supplied with Device Support Adapter materials that allow the user to properly support and stabilize a 2.5-inch or 3.5-inch form-factor device while under test.

Figure 16, later within this document, illustrates the installation and a typical application of the Device Support Adapter materials.

General Test Adapter, Cable, and Connector

Observing simple precautions can ensure accurate and reliable measurements.

Handling and Storage

Before each use of the 8639G4-TPA, ensure that all connectors are clean. Handle all cables carefully and store the 8639G4-TPA in the foam-lined instrument case when not in use, if possible. Do not set connectors contact end down. Install the SMA protective end caps when the 8639G4-TPA is not in use.

Visual Inspection

Be sure to inspect all cables carefully before making a connection. Inspect all cables for metal particles, scratches, deformed threads, dents, or bent, broken, or misaligned center conductors. Do not use damaged cables.

Cleaning

If necessary, clean the connectors using low-pressure (less than 60 PSI) compressed air or nitrogen with an effective oil-vapor filter and condensation trap. Clean the cable threads, if necessary, using a lint-free swab or cleaning cloth moistened with isopropyl alcohol. Always completely dry a connector before use. Do not use abrasives to clean the connectors. Re-inspect connectors, making sure no particles or residue remains.

Making Connections

Before making any connections, review the “Care and Handling Precautions” section. Follow these guidelines when making connections:

- Align cables carefully
- Make preliminary connection lightly
- To tighten, turn connector nut only
- Do not apply bending force to cable
- Do not over-tighten preliminary connections
- Do not twist or screw-in cables
- Use an appropriately sized torque wrench (depends on SMA gender), and do not tighten past the “break” point of the torque wrench (normally set to 5 in-lbs)

Electrostatic Discharge Information

Protection against electrostatic discharge (ESD) is essential while connecting, inspecting, or cleaning the 8639G4-TPA test adapter and connectors attached to a static-sensitive circuit (such as those found in test sets).

Electrostatic discharge can damage or destroy electronic components. Be sure to perform all work on electronic assemblies at a static-safe workstation, using two types of ESD protection:

- Conductive table-mat and wrist-strap combination
- Conductive floor-mat and heel-strap combination

When used together, both of these types provide a significant level of ESD protection. Used alone, the table-mat and wrist-strap combination provide adequate ESD protection. To ensure user safety, the static-safe accessories must provide at least 1 MΩ of isolation from ground. Acceptable ESD accessories may be purchased from a local supplier.

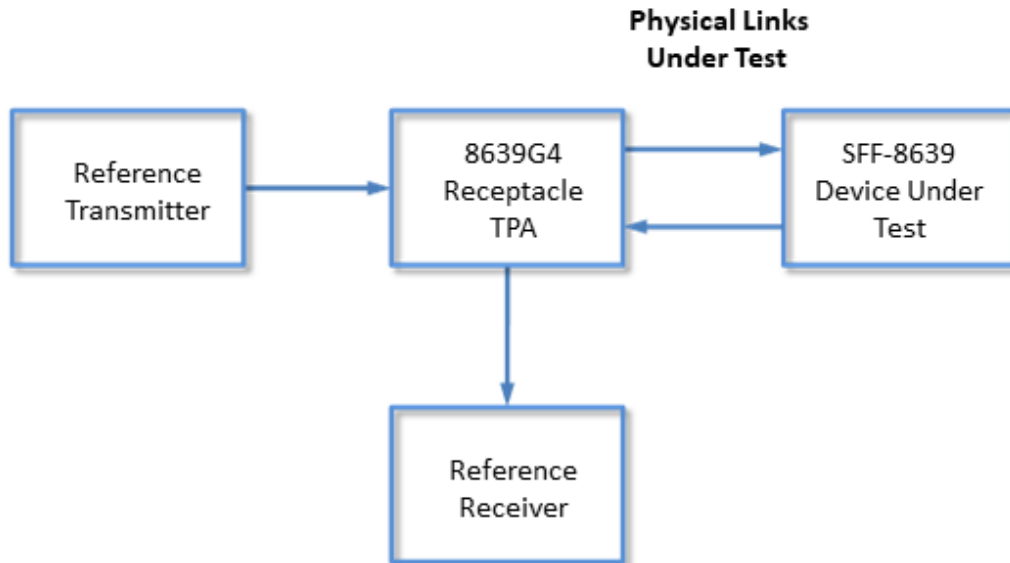
WARNING: These techniques for a static-safe workstation should not be used when working on circuitry with a voltage potential greater than 500 volts.

User Model

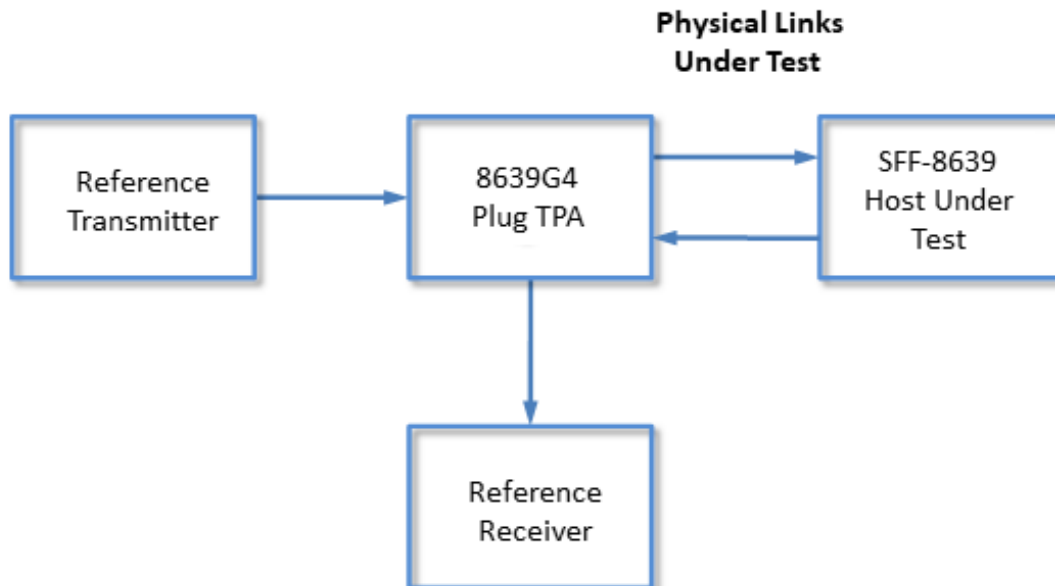
The 8639G4-TPA supports all testing of SFF-8639 Gen-4 related interface specifications such as PCIe SFF-8639, SATA Express, MultiLink SAS, and others. It is capable of performing beyond the scope of measurements required, limited only by the specifications, environmental, care and handling as stated in this document.

The following examples are suggestions for possible testing setups.

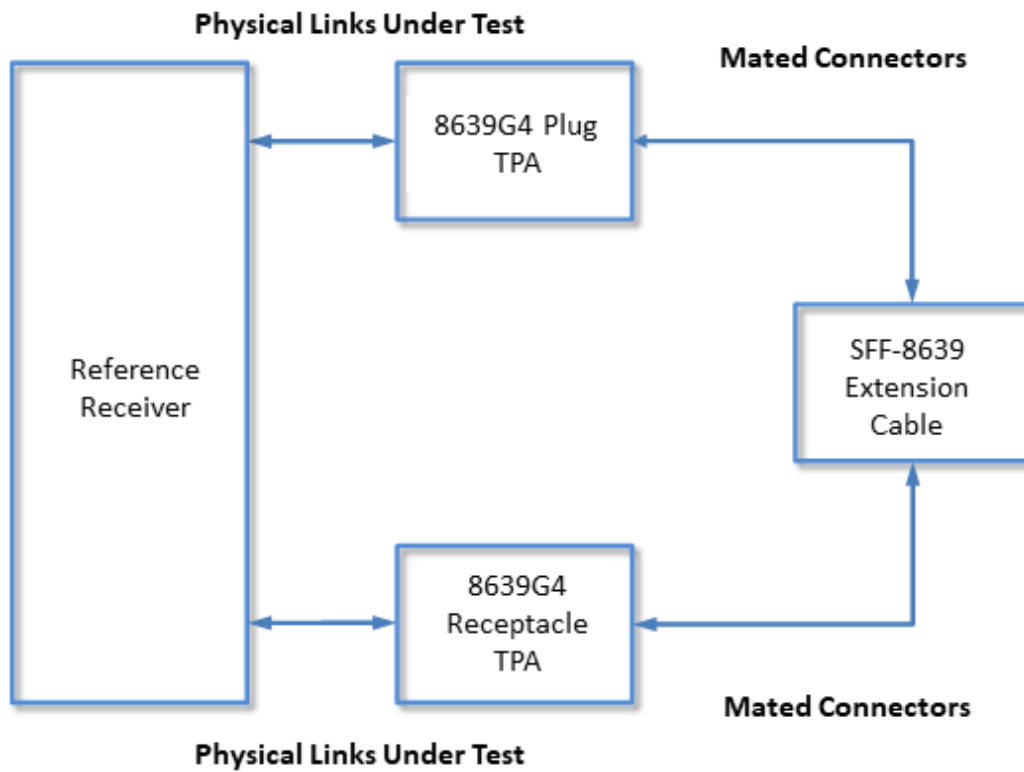
In this first example, an 8639 Gen-4 Receptacle TPA is used to test an 8639 device:



The second example shows an 8639 Gen-4 Plug TPA used to test a host:



The third example shows one 8639 Gen-4 Plug TPA and one 8639 Gen-4 Receptacle TPA used for testing a 8639 extension cable:



Calibration Through De-Embedding

The SFF-8639 Gen-4 Host and Device Test Adapters are fully passive components. Therefore, calibration compensating for the losses must occur within the test instrumentation that drives the SFF-8639 receiver or looks at the response of the SFF-8639 transmitter.

The 8639G4-TPAs have Touchstone S4P files for de-embedding the electrical length and losses within the TPA up to the SFF-8639 Gen-4 connector interface pads. (Contact Wilder Technologies, support@wilder-tech.com, to obtain a copy of the S4P files.) The Touchstone S4P files enable the test engineer to compensate for the last four of the following six repeatable, systematic errors that occur when moving the reference plane:

- Signal leakage effects: *Directivity errors*
- Signal leakage effects: *Crosstalk errors*
- Reflection effects: *Source Impedance Mismatching errors*
- Reflection effects: *Load Impedance Mismatching errors*
- Bandwidth effects: *Receiver Transmission in Test Equipment errors*
- Bandwidth effects: *Receiver Reflection-tracking in Test Equipment errors*

These errors are corrected on each port. Refer to the Instrument Manual for instructions on the instrument's specific de-embedding process.

NOTE: The reference plane is the boundary, both physically and electrically, between the calibrated and un-calibrated portions of the circuit. Everything outside the reference plane is considered part of the DUT. Any instrument that does not use calibration or de-embedding of the test fixture defines the DUT as the total of externally connected components. If the de-embedding file is not used, all of the 8639G4-TPA and associated coaxial cables, as well as cables connecting the TPA assembly to the test instrument, would be a part of the DUT.

Non-repeatable errors, such as drift or random errors, can be reduced but not corrected. Drift errors aggregate over time or with environmental changes such as temperature shift. To eliminate drift errors, perform an instrumentation-level calibration.

A random error cannot be corrected through calibration since the error occurred randomly. Random errors are typically associated with either test instrument noise or test repeatability problems. Reduce test instrument noise by increasing source power, lowering the IF bandwidth, or averaging results over multiple sweeps. Reduce test repeatability problems through the use of a torque wrench or, again, by averaging over multiple sweeps.

Mechanical and Environmental Specifications

NOTE: All specifications in this manual are subject to change.

Table 1. General Specifications

ITEM	DESCRIPTION
Usage Environment	Controlled indoor environment
Plug Test Adapter Length (w/standard cables)	246 mm +/- 2 mm (9.70 inches +/- .08 inches) (Characteristic)
Receptacle Test Adapter Length (w/std. cables)	381 mm +/- 2 mm (15.00 inches +/- .08 inches) (Characteristic)
Operating Temperature	0°C to +55°C (32°F to +131°F) (Characteristic)
Storage Temperature	-40°C to +70°C (-40°F to +158°F) (Characteristic)

8639G4-TPA-R Cable Pinout

The 8639G4-TPA-R cables provide 28 SMA connectors (access up to six lanes of differential TX and RX, and up to two differential reference clocks), one 4-position power connector, and one 16-position alternate connector. Labels clearly mark each cable or connector. The following figure refers to pin-description tables for each of the three connector types. Note: The power supplies each have 22 μ F in parallel with a 0.01 μ F capacitor, with the exception of the +3.3V, which does not have the 22 μ F cap. The pre-charge signals each have a series 2 Ohm resistor to their respective power supplies.

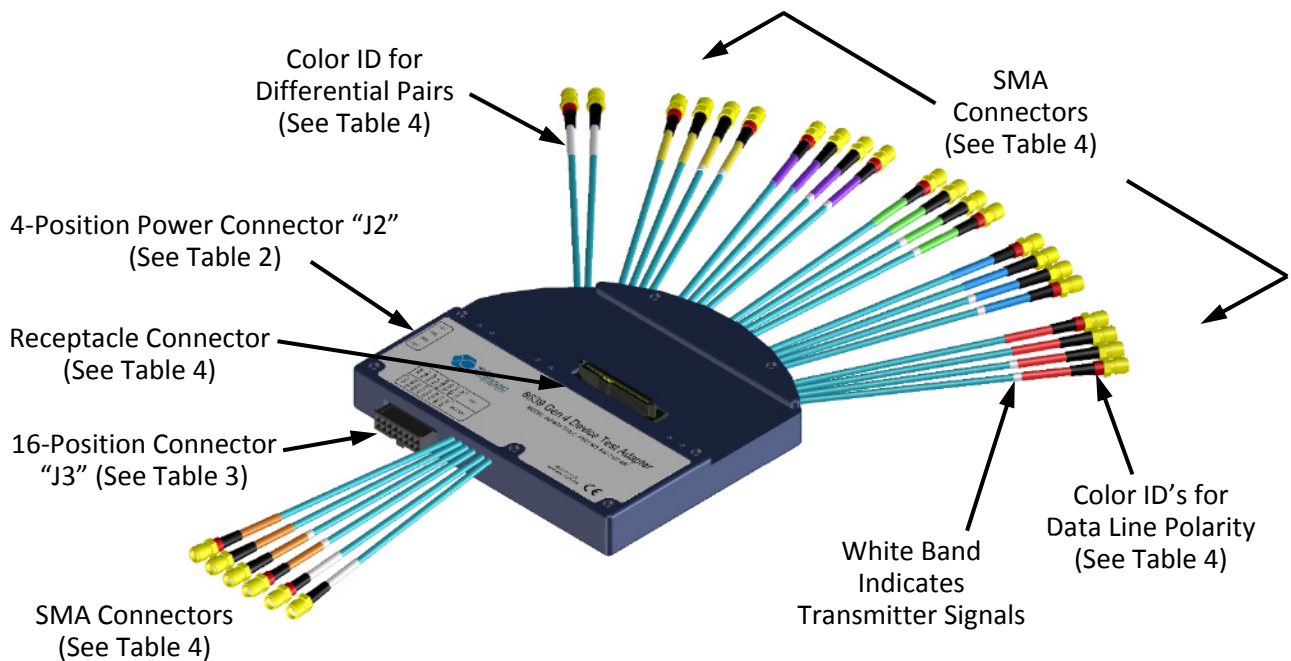


Figure 4. Cable Connectors ("Universal" 8639G4-TPA-R shown)

Table 2. 8639G4-TPA-R 4-Position Power Connector “J2”

LABEL	PIN NO.	DESCRIPTION
+12V	Pin 1	+12 Volts
GND	Pin 2	Power Ground
GND	Pin 3	Power Ground
+5V	Pin 4	+5 Volts

Table 3. 8639G4-TPA-R 16-Position Alternate Connector “J3” (“Universal” 8639G4-TPA-R Described)

LABEL	PIN NO.	DESCRIPTION
GND	Pin 1	Power Ground
PERST#	Pin 2	PCI Express Reset (Port A)
WAKE#	Pin 3	Wake (required only if the device/system supports wake-up and/or the OBFF mechanism)
PIN P2	Pin 4	Access to SFF-8639 Gen-4 Connector Pin P2 (description is interface type dependent)
PIN P3	Pin 5	Access to Power Disable or PCIe Reference Clock Request/Device Sleep for SATA Express Only
PRSNT#	Pin 6	Device Present (PCI Express SFF-8639 module presence detect pin)
ACTIVY#	Pin 7	PCI Express Activity (indicates read or write activity of the SFF-8639 module)
DLEN#	Pin 8	PCI Express Dual Link Enable
+3.3V	Pin 9	+3.3 Volts
PIN E4	Pin 10	Access to Clock Request/PCIe Reset for Port B
RES E6	Pin 11	Access to “Reserved” SFF-8639 Connector Pin E6 (description is interface type dependent)
RES E16	Pin 12	Access to “Reserved” SFF-8639 Connector Pin E16 (description is interface type dependent)
RES S15	Pin 13	Access to “Reserved” SFF-8639 Connector Pin S15 (description is interface type dependent)
IFDET#	Pin 14	Interface Type Detect (PCI Express SFF-8639 module presence detect pin)
SMCLK	Pin 15	SMBus (System Management Bus) Clock
SMDAT	Pin 16	SMBus (System Management Bus) Data

Table 4. 8639 Gen-4 Receptacle Pin Assignments on notched side of connector
















Pin Description	Connector Pin Number	Destination Name	Color ID for Data Line Polarity	Color ID for Differential Pair (Receptacle)	
Signal Ground	S1	Signal Ground, GND	N/A	N/A	
Device SAS/SATA 0 Receiver Positive	S2	DEV S0R+	Red	Orange	
Device SAS/SATA 0 Receiver Negative	S3	DEV S0R -	Black	Orange	
Signal Ground	S4	Signal Ground, GND	N/A	N/A	
Device SAS/SATA 0 Transmitter Negative	S5	DEV S0T-	Black	Orange/Wht Band	
Device SAS/SATA 0 Transmitter Positive	S6	DEV S0T+	Red	Orange/Wht Band	
Signal Ground	S7	Signal Ground, GND	N/A	N/A	
PCIe Ref Clock for Port B Positive	E1	DEV RCLKB+	Red	White	
PCIe Ref Clock for Port B Negative	E2	DEV RCLKB-	Black	White	
+3.3 Volts for SM Bus	E3	+3.3V	Black	N/A	
Clock Request/PCIe Reset for Port B	E4	PIN E4 (CLKREQ#/PERSTB#)	N/A	N/A	
PCIe reset for Port A	E5	PERST#	N/A	N/A	
Reserved	E6	RES E6	N/A	N/A	
Device/System Specific Wake-Up	P1	WAKE#	N/A	N/A	
8639 Gen-4 Connector Pin P2	P2	PIN P2	N/A	N/A	
Power Disable or PCIe Reference Clock Request/Device Sleep for SATA Express Only	P3	PIN P3 (PWRDIS/CLKREQ#/DEVSLP)	N/A	N/A	
Interface Type Detect	P4	IFDET#	N/A	N/A	
Power Ground	P5, P6	GND	N/A	N/A	
+5 Volts pre-charge	P7	2 Ohm Resistor to +5V	N/A	N/A	
+5 Volts	P8, P9	+5V	N/A	N/A	
Device Present	P10	PRSNT#	N/A	N/A	
PCIe Activity	P11	ACTIVY#	N/A	N/A	
Power Ground	P12	GND	N/A	N/A	
+12 Volts pre-charge	P13	2 Ohm Resistor to +12V	N/A	N/A	
+12 Volts	P14, P15	+12V	N/A	N/A	

Table 4. 8639 Gen-4 Receptacle Pin Assignments on side opposed to notch side of connector

Pin Description	Connector Pin Number	Destination Name	Color ID for Data Line Polarity	Color ID for Differential Pair (Plug)
PCIe Ref Clock for Port A Positive	E7	DEV RCLKA+	Red	White
PCIe Ref Clock for Port A Negative	E8	DEV RCLKB-	Black	White
Signal Ground	E9	Signal Ground, GND	N/A	N/A
Device PCIe 0 Receiver Positive	E10	DEV PER0+	Red	Yellow
Device PCIe 0 Receiver Negative	E11	DEV PER0-	Black	Yellow
Signal Ground	E12	Signal Ground, GND	N/A	N/A
Device PCIe 0 Transmitter Negative	E13	DEV PET0-	Black	Yellow/Wht Band
Device PCIe 0 Transmitter Positive	E14	DEV PET0+	Red	Yellow/Wht Band
Signal Ground	E15	Signal Ground, GND	N/A	N/A
Reserved	E16	RES E16	N/A	N/A
Signal Ground	S8	Signal Ground, GND	N/A	N/A
Device SAS 1 Receiver Positive	S9	DEV S1R+	Red	Violet
Device SAS 1 Receiver Negative	S10	DEV S1R -	Black	Violet
Signal Ground	S11	Signal Ground, GND	N/A	N/A
Device SAS 1 Transmitter Negative	S12	DEV S1T-	Black	Violet/Wht Band
Device SAS 1 Transmitter Positive	S13	DEV S1T+	Red	Violet/Wht Band
Signal Ground	S14	Signal Ground, GND	N/A	N/A
Reserved	S15	RES S15	N/A	N/A
Signal Ground	S16	Signal Ground, GND	N/A	N/A
Device PCIe 1 Receiver Positive	S17	DEV PER1+	Red	Green
Device PCIe 1 Receiver Negative	S18	DEV PER1-	Black	Green
Signal Ground	S19	Signal Ground, GND	N/A	N/A
Device PCIe 1 Transmitter Negative	S20	DEV PET1-	Black	Green/Wht Band
Device PCIe 1 Transmitter Positive	S21	DEV PET1+	Red	Green/Wht Band
Signal Ground	S22	Signal Ground, GND	N/A	N/A



Table 4. 8639 Gen-4 Receptacle Pin Assignments on side opposed to notch side of connector (continued)

Pin Description	Connector Pin Number	Destination Name	Color ID for Data Line Polarity	Color ID for Differential Pair (Plug)	
Device PCIe 2 Receiver Positive	S23	DEV PER2+	Red	Blue	
Device PCIe 2 Receiver Negative	S24	DEV PER2-	Black	Blue	
Signal Ground	S25	Signal Ground, GND	N/A	N/A	
Device PCIe 2 Transmitter Negative	S26	DEV PET2-	Black	Blue/Wht Band	
Device PCIe 2 Transmitter Positive	S27	DEV PET2+	Red	Blue/Wht Band	
Signal Ground	S28	Signal Ground, GND	N/A	N/A	
Device PCIe 3 Receiver Positive	E17	DEV PER3+	Red	Red	
Device PCIe 3 Receiver Negative	E18	DEV PER3-	Black	Red	
Signal Ground	E19	Signal Ground, GND	N/A	N/A	
Device PCIe 3 Transmitter Negative	E20	DEV PET3-	Black	Red/Wht Band	
Device PCIe 3 Transmitter Positive	E21	DEV PET3+	Red	Red/Wht Band	
Signal Ground	E22	Signal Ground, GND	N/A	N/A	
SM-Bus Clock	E23	SMCLK	N/A	N/A	
SM-Bus Data	E24	SMDAT	N/A	N/A	
PCIe Dual Link Enable	E25	DLEN#	N/A	N/A	

8639G4-TPA-P Cable Pin-out

The 8639G4-TPA-P cables provide 28 SMA connectors (access up to six lanes of PCIe differential TX and RX, and up to two differential reference clocks) and one 10-Position low-speed connector. Labels clearly mark each cable or connector. The following figure refers to the pin-description table for the plug connector.

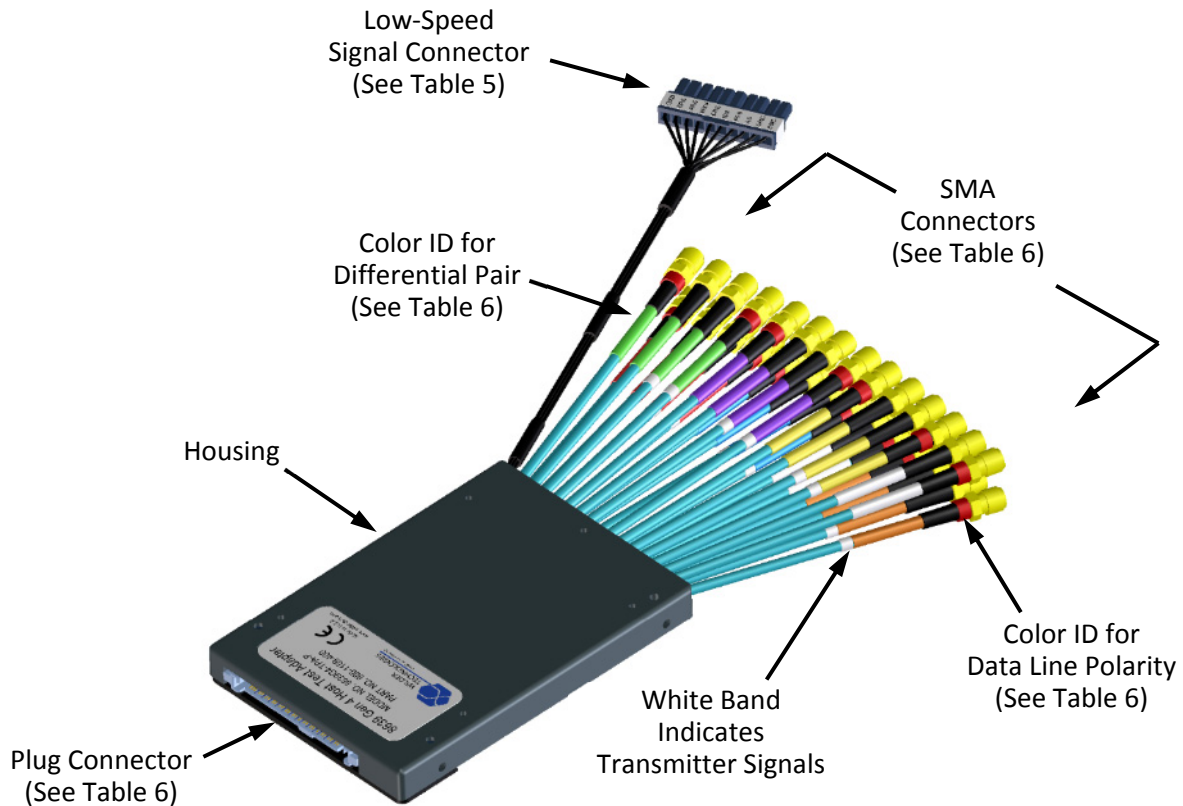


Figure 5. Cable Connectors ("Universal" 8639G4-TPA-P shown)

Table 5. 8639G4-TPA-P 10-Position Low-Speed Connector “J3”

LABEL	PIN NO.	DESCRIPTION
GND	Pin 1	Power Ground
BRS	Pin 2	PCI Express Reset (Port B) or Clock Request
ARS	Pin 3	PCI Express Reset (Port A)
DRS	Pin 4	Access to 8639 Connector P2 (description is interface type dependent)
WK#	Pin 5	Device/System Specific Wake-Up
ID#	Pin 6	PCI Express Interface Type Detect
PR#	Pin 7	PCI Express Device Present
AS	Pin 8	PCI Express Activity
SMC	Pin 9	SMBus (System Management Bus) Clock
SMD	Pin 10	SMBus (System Management Bus) Data

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Table 6. 8639 Gen-4 Plug Pin Assignments on keyed side of connector

Pin Description	Connector Pin Number	Destination Name	Color ID for Data Line Polarity	Color ID for Differential Pair (Receptacle)
Signal Ground	S1	Signal Ground, GND	N/A	N/A
Host SAS/SATA 0 Transmitter Positive	S2	HOST S0T+	Red	Orange/Wht Band
Host SAS/SATA 0 Transmitter Negative	S3	HOST S0T -	Black	Orange/Wht Band
Signal Ground	S4	Signal Ground, GND	N/A	N/A
Host SAS/SATA 0 Receiver Negative	S5	HOST S0R-	Black	Orange
Host SAS/SATA 0 Receiver Positive	S6	HOST S0R+	Red	Orange
Signal Ground	S7	Signal Ground, GND	N/A	N/A
PCIe Ref Clock for Port B Positive	E1	HOST RCLKB+	Red	White
PCIe Ref Clock for Port B Negative	E2	HOST RCLKB-	Black	White
+3.3 Volts for SM Bus	E3	0.01 uF bypass to GND	Black	N/A
Clock Request/PCIe Reset for Port B	E4	BRS	N/A	N/A
PCIe Reset for Port A	E5	ARS	N/A	N/A
Reserved	E6	No connection	N/A	N/A
Device/System Specific Wake-Up	P1	WK#	N/A	N/A
8639 Gen-4 Connector Pin P2	P2	DRS	N/A	N/A
Power Disable or PCIe Reference Clock Request/Device Sleep for SATA Express Only	P3	No connection	N/A	N/A
Interface Type Detect	P4	ID#	N/A	N/A
Power Ground	P5, P6	GND	N/A	N/A
+5 Volts precharge	P7	No connection	N/A	N/A
+5 Volts	P8, P9	No connection	N/A	N/A
Device Present	P10	PR#	N/A	N/A
PCIe Activity	P11	AS	N/A	N/A
Power Ground	P12	GND	N/A	N/A
+12 Volts precharge	P13	No connection	N/A	N/A
+12 Volts	P14, P15	No connection	N/A	N/A

Table 6. 8639 Gen-4 Plug Pin Assignments on side opposed to keyed side of connector

Pin Description	Connector Pin Number	Destination Name	Color ID for Data Line Polarity	Color ID for Differential Pair (Plug)
PCIe Ref Clock for Port A Positive	E7	HOST RCLKA+	Red	White
PCIe Ref Clock for Port A Negative	E8	HOST RCLKA-	Black	White
Signal Ground	E9	Signal Ground, GND	N/A	N/A
Host PCIe 0 Transmitter Positive	E10	HOST PET0+	Red	Yellow/Wht Band
Host PCIe 0 Transmitter Negative	E11	HOST PET0-	Black	Yellow/Wht Band
Signal Ground	E12	Signal Ground, GND	N/A	N/A
Host PCIe 0 Receiver Negative	E13	HOST PER0-	Black	Yellow
Host PCIe 0 Receiver Positive	E14	HOST PER0+	Red	Yellow
Signal Ground	E15	Signal Ground, GND	N/A	N/A
Reserved	E16	No connection	N/A	N/A
Signal Ground	S8	Signal Ground, GND	N/A	N/A
Host SAS 1 Transmitter Positive	S9	HOST S1T+	Red	Violet/Wht Band
Host SAS 1 Transmitter Negative	S10	HOST S1T -	Black	Violet/Wht Band
Signal Ground	S11	Signal Ground, GND	N/A	N/A
Host SAS 1 Receiver Negative	S12	HOST S1R-	Black	Violet
Host SAS 1 Receiver Positive	S13	HOST S1R+	Red	Violet
Signal Ground	S14	Signal Ground, GND	N/A	N/A
Reserved	S15	No connection	N/A	N/A
Signal Ground	S16	Signal Ground, GND	N/A	N/A
Host PCIe 1 Transmitter Positive	S17	HOST PET1+	Red	Green/Wht Band
Host PCIe 1 Transmitter Negative	S18	HOST PET1-	Black	Green/Wht Band
Signal Ground	S19	Signal Ground, GND	N/A	N/A
Host PCIe 1 Receiver Negative	S20	HOST PER1-	Black	Green
Host PCIe 1 Receiver Positive	S21	HOST PER1+	Red	Green
Signal Ground	S22	Signal Ground, GND	N/A	N/A

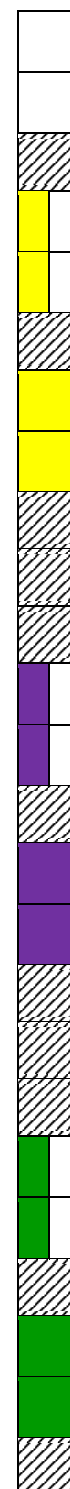
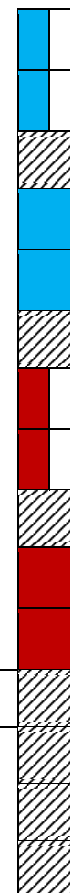


Table 6. 8639 Gen-4 Plug Pin Assignments on side opposed to keyed side of connector (continued)

Pin Description	Connector Pin Number	Destination Name	Color ID for Data Line Polarity	Color ID for Differential Pair (Plug)
Host PCIe 2 Transmitter Positive	S23	HOST PET2+	Red	Blue/Wht Band
Host PCIe 2 Transmitter Negative	S24	HOST PET2-	Black	Blue/Wht Band
Signal Ground	S25	Signal Ground, GND	N/A	N/A
Host PCIe 2 Receiver Negative	S26	HOST PER2-	Black	Blue
Host PCIe 2 Receiver Positive	S27	HOST PER2+	Red	Blue
Signal Ground	S28	Signal Ground, GND	N/A	N/A
Host PCIe 3 Transmitter Positive	E17	HOST PET3+	Red	Red/Wht Band
Host PCIe 3 Transmitter Negative	E18	HOST PET3-	Black	Red/Wht Band
Signal Ground	E19	Signal Ground, GND	N/A	N/A
Host PCIe 3 Receiver Negative	E20	HOST PER3-	Black	Red
Host PCIe 3 Receiver Positive	E21	HOST PER3+	Red	Red
Signal Ground	E22	Signal Ground, GND	N/A	N/A
SM-Bus Clock	E23	SMC	N/A	N/A
SM-Bus Data	E24	SMD	N/A	N/A
PCIe Dual Link Enable	E25	No connection	N/A	N/A



8639 Gen-4 Configuration Board

When used with the 8639G4-TPA-P (Host Test Adapter), the 8639 Gen-4 Configuration Board provides access to IFDET# (P4) and PRSNT# (P10) signals. The use of the combined signals provides the ability to set and detect the appropriate device type (configuration). Jumper configurations are referenced and clearly marked on the board.

The 8639 Gen-4 Configuration Board also provides access to other low-speed signals as well as jumper access for the WAKE# signal. Momentary switches allow the user to reset each of the three “RESET” signal functions. Specific features and usage models are presented within Addendum A and B of this document.

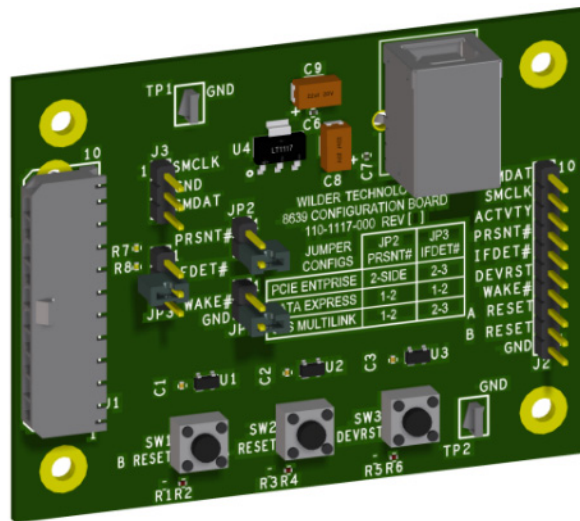


Figure 6. 8639 Gen-4 Configuration Board

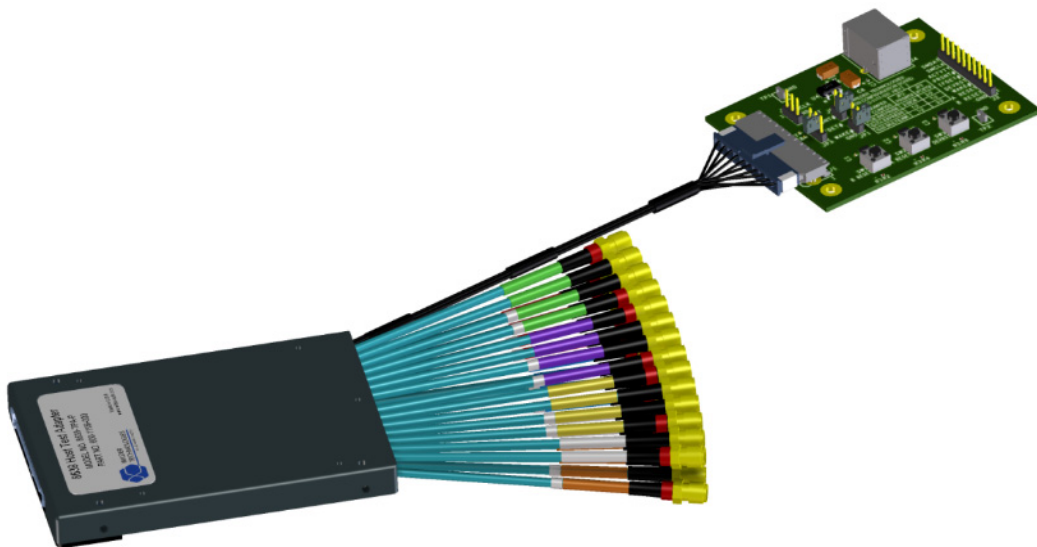


Figure 7. 8639 Gen-4 Configuration Board mated to an 8639G4-TPA-P (Plug) Test Adapter

Electrical Specifications

NOTE: All specifications in this manual are subject to change.

Table 7. Electrical Specifications

SPECIFICATION	MINIMUM	TYPICAL	MAXIMUM	NOTES
Differential Impedance (ohms), 70 ps Rise Time, 20 – 80 percent	94		106	All Differential Pairs, Receptacle and Plug, excluding 8639 Gen-4 connectors.
Differential Impedance (ohms), 70 ps Rise Time, 20 – 80 percent	>92		106	All Differential Pairs, Receptacle and Plug, including 8639 Gen-4 connectors.
Impedance (ohms), 70ps Rise Time, 20 – 80 percent	47		53	All Differential Pairs, Receptacle and Plug, excluding 8639 Gen-4 connectors.
Intra-pair Skew (ps)		<2.5		All Differential Pairs, Receptacle and Plug.
Inter-pair Skew (ps)		< ± 4.5		All Differential Pairs, Receptacle and Plug.
NEXT at 10 GHz		Better Than -32dB		All adjacent differential pairs, single aggressor, with 8639 Gen-4 connectors.
FEXT at 10 GHz Mated TPAs w/ 8639 Gen-4 Connector		Better Than -35dB		All adjacent differential pairs, single aggressor, with 8639 Gen-4 connectors.
Current Carrying (A) Per Pin			1.5	+5V, and +12V Power.
Current Carrying (mA)			100	+3.3V Power.

Note: The following Eye-Diagrams and S-Parameter Plots were measured and plotted without de-embedding except for Insertion Loss (IL) where de-embedding was applied to the measurement to render the following IL plot. This is due to loss by the trace length on the SFF-8639G4 Gen-4 TPAs and therefore referring to the PCI Express SFF-8639G4 Module Specification, Revision 4.0, Version 0.9 October 27, 2020 section 5.2.4 Test Fixture Requirements: Bullet 6, test fixture de-embedding was applied.

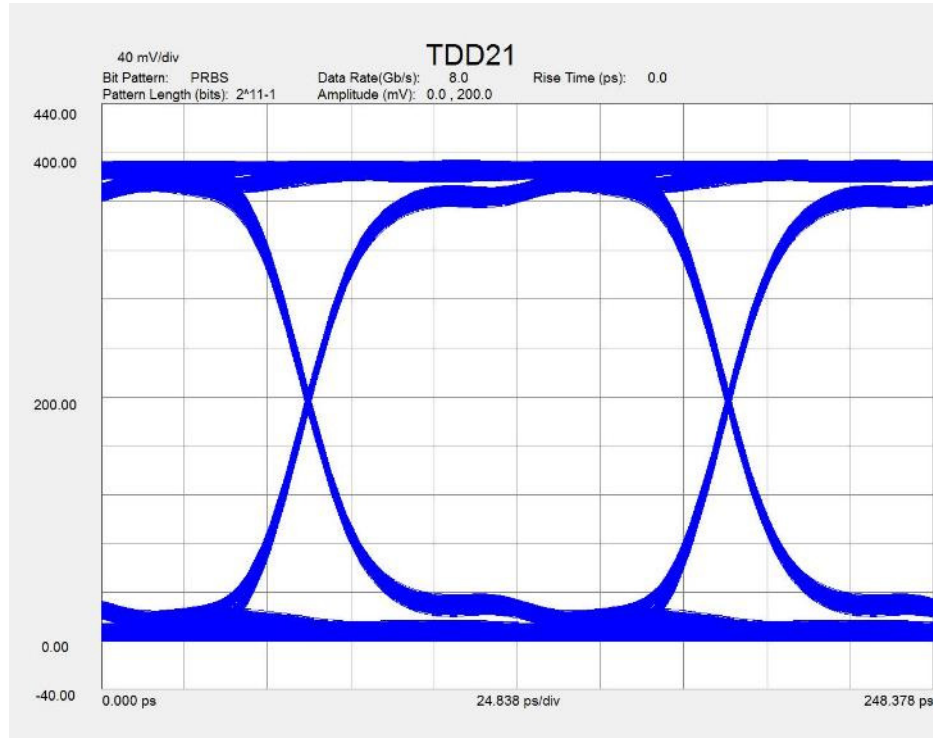


Figure 8. Typical mated pair 8 Gb/s eye diagram, without de-embedding

Name	Result
Eye Level Zero (mV):	16.4475
Eye Level One (mV):	376.7832
Eye Level Mean (mV):	196.6153
Eye Amplitude (mV):	360.3356
Eye Height (mV):	300.0851
Eye Height (dB):	-2.4963
Eye Width:	121.9153
Eye Opening Factor:	0.8328
Eye Signal to Noise:	17.9419
Eye Duty Cycle Dist:	0.0155
Eye Duty Cycle Dist (%):	0.0124
Eye Rise Time (10-90):	38.8337
Eye Fall Time (10-90):	38.7988
Eye Jitter (PP):	2.1588
Eye Jitter (RMS):	0.6143

Figure 9. Typical mated pair 8 Gb/s eye data, without de-embedding

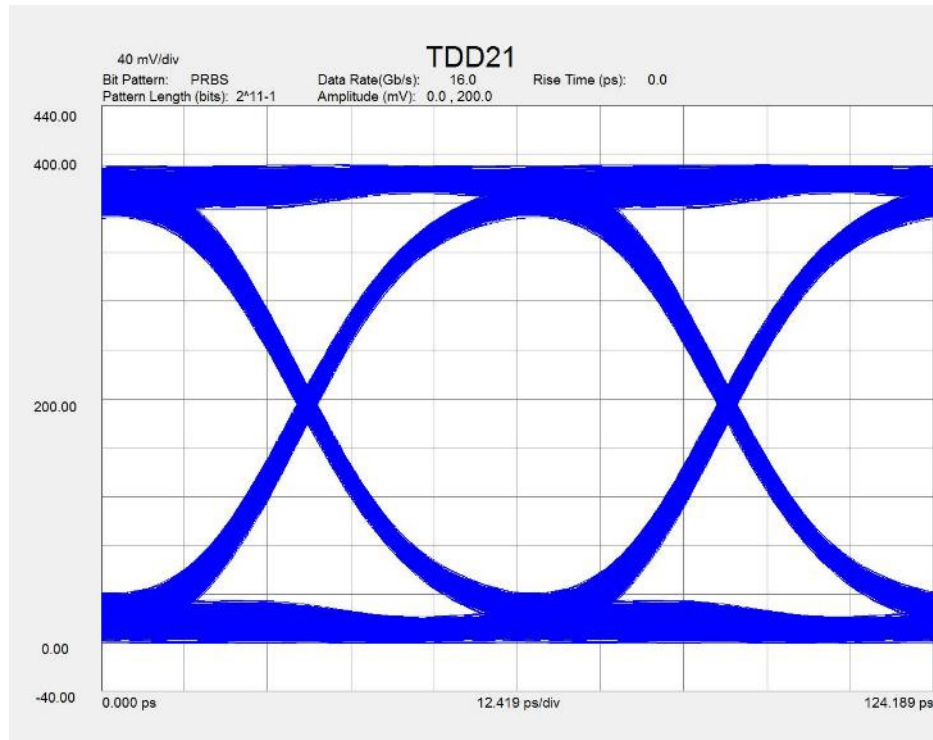


Figure 10. Typical mated pair 16 Gb/s eye diagram without de-embedding

Parameter Measurement Result	
Name	Result
Eye Level Zero (mV):	22.3469
Eye Level One (mV):	368.4293
Eye Level Mean (mV):	195.3881
Eye Amplitude (mV):	346.0824
Eye Height (mV):	278.7662
Eye Height (dB):	-3.1364
Eye Width:	57.5795
Eye Opening Factor:	0.8055
Eye Signal to Noise:	15.4235
Eye Duty Cycle Dist:	0.0133
Eye Duty Cycle Dist (%):	0.0213
Eye Rise Time (10-90):	35.5555
Eye Fall Time (10-90):	35.5609
Eye Jitter (PP):	3.4180
Eye Jitter (RMS):	0.8519

Figure 11. Typical mated pair 16 Gb/s eye data, without de-embedding

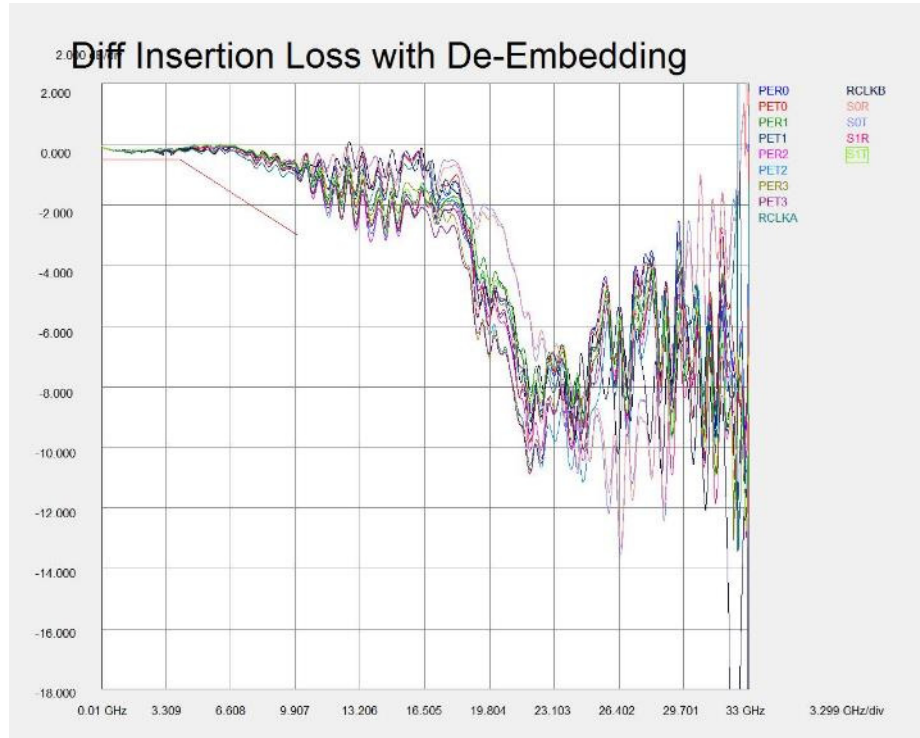


Figure 12. Typical mated pair balanced insertion loss, with de-embedding

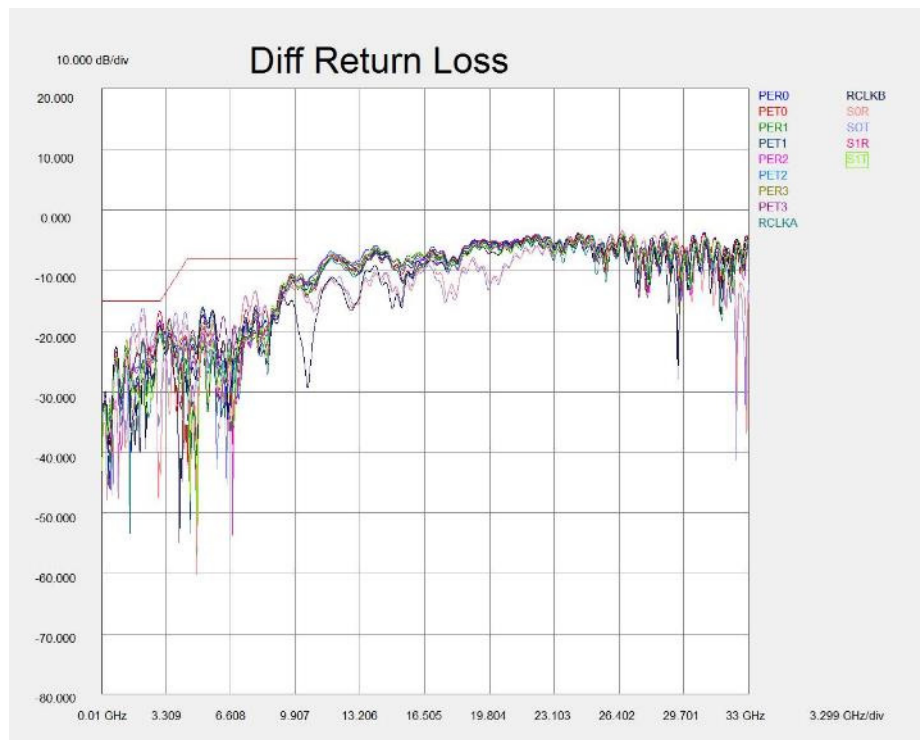


Figure 13. Typical mated pair balanced return loss, without de-embedding

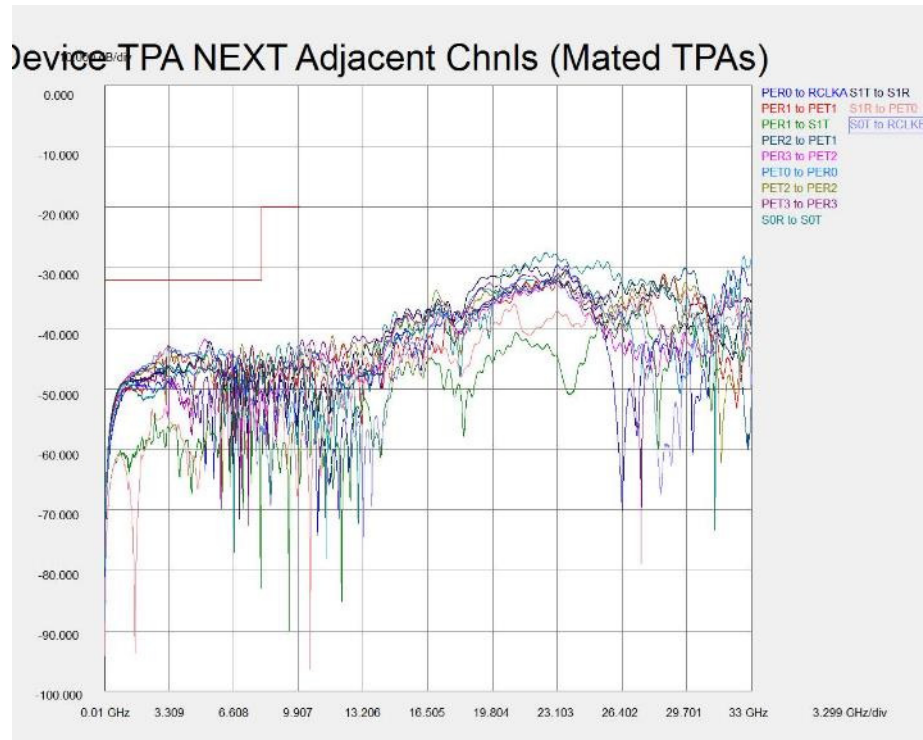


Figure 14. Typical Device (Plug TPA) side NEXT, adjacent differential pairs, without de-embedding

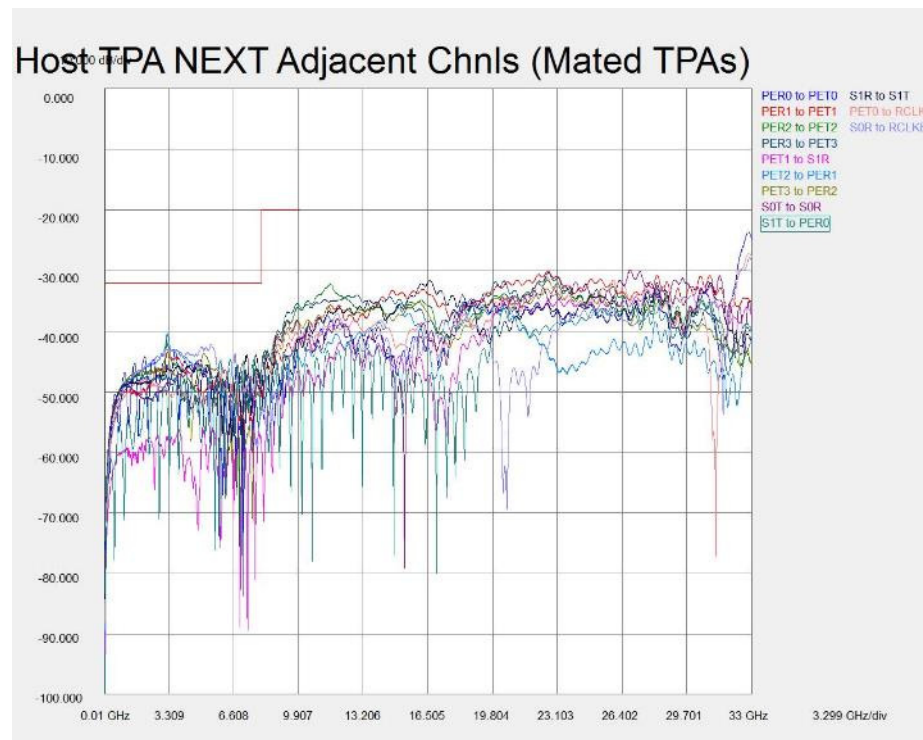


Figure 15. Typical Host (Receptacle TPA) side NEXT, adjacent differential pairs, without de-embedding

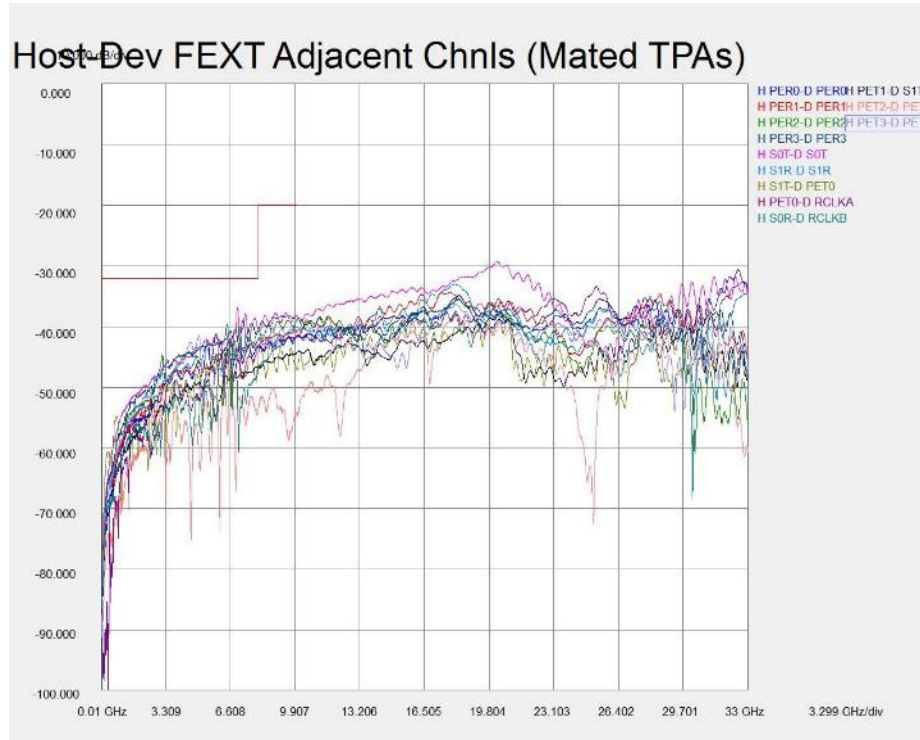


Figure 16. Typical Differential FEXT with mated connectors, adjacent differential pairs, without de-embedding

8639G4-TPA-R Accessories

The 8639G4-TPA-R (Device TPA) is supplied with Disk Support Adapter materials that allow the user to properly support and stabilize a 2.5 or 3.5-inch form-factor disk drive while under test.

The figure, below, illustrates the installation and a typical application of the Disk Support Adapter materials.

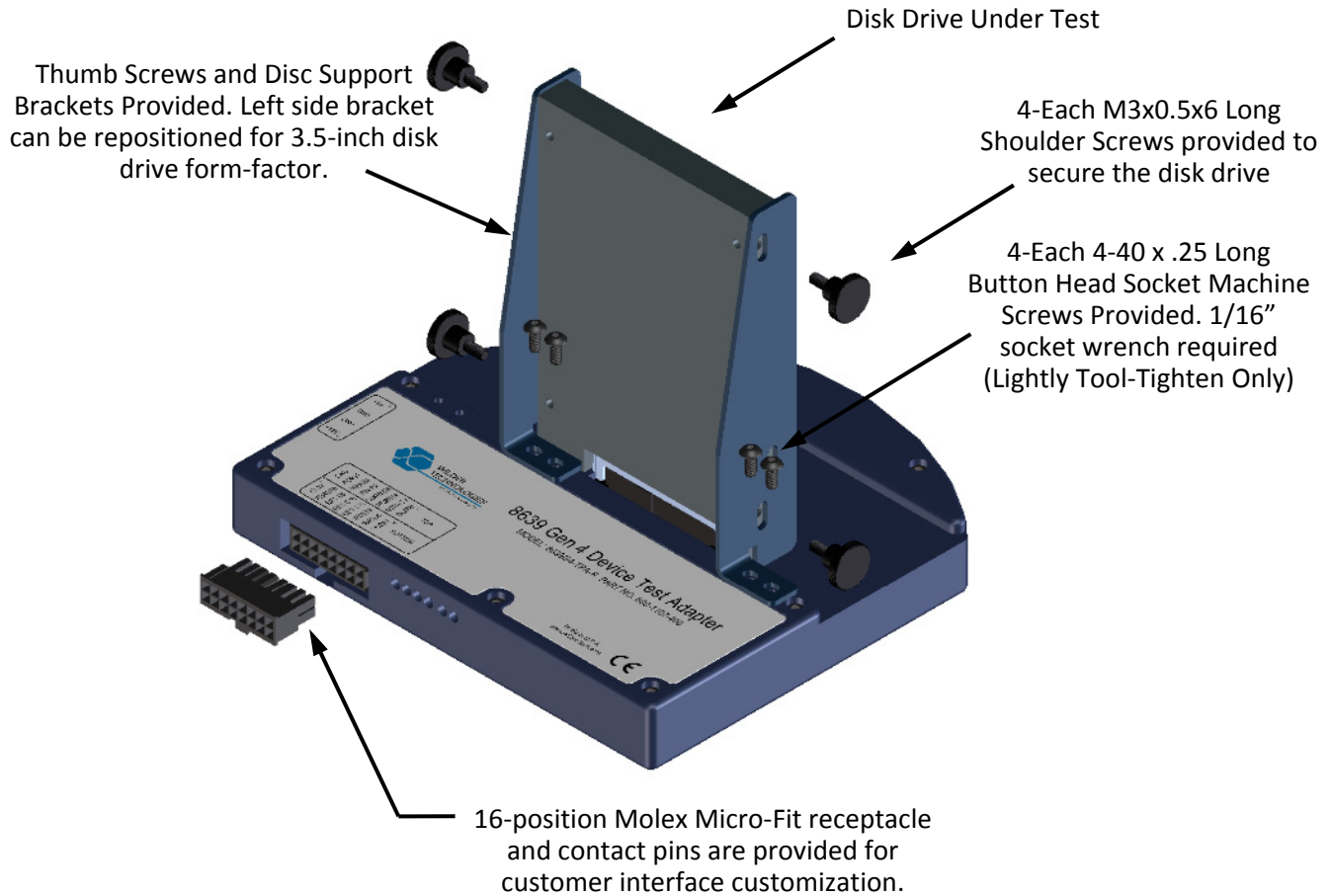


Figure 17. 8639G4-TPA-R Device Support Adapter (Shown without High Speed Cables for Clarity)

Compliance with Environmental Legislation

Wilder Technologies, LLC, is dedicated to complying with the requirements of all applicable environmental legislation and regulations, including appropriate recycling and/or disposal of our products.



WEEE Compliance Statement

The European Union adopted Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE), with requirements that went into effect August 13, 2005. WEEE is intended to reduce the disposal of waste from electrical and electronic equipment by establishing guidelines for prevention, reuse, recycling and recovery.

Wilder Technologies has practices and processes in place to conform to the requirements in this important Directive.

In support of our environmental goals, effective January 1st, 2009 Wilder Technologies, LLC has partnered with EG Metals Inc. – Metal and Electronics Recycling of Hillsboro, Oregon, www.egmetalrecycling.com, to recycle our obsolete and electronic waste in accordance with the European Union Directive 2002/96/EC on waste electrical and electronic equipment ("WEEE Directive").

As a service to our customers, Wilder Technologies is also available for managing the proper recycling and/or disposal of all Wilder Technologies products that have reached the end of their useful life. For further information and return instructions, contact support@wilder-tech.com.



Compliance to RoHS 2 Substance Restrictions

Wilder Technologies, LLC certifies that the parts described in this document are compliant to the substance restrictions of Directive 2011/65/EU and Amendment Directive (EU) 2015/863 of the European Parliament, and of the Council of 8 June, 2011 and 31 March, 2015 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS 2 Directive), prohibiting the use in homogeneous materials in excess of the listed maximum concentration value, except in cases where use is allowed by applicable exemptions listed in Annex III and Annex IV of the Directive.

Compliance with RoHS 2 has been verified through internal controls at design and production sites, including establishment of processes for specifying and controlling materials and segregation of non-compliant parts, receipt of supplier declarations of compliance and/or analytical test.

Glossary of Terms

TERMINOLOGY	DEFINITION
Aggressor	A signal imposed on a system (i.e., cable assembly) to measure response on other signal carriers.
Decibel (dB)	Ten times the common logarithm (i.e. log10) of the ratio of relative powers.
Informative	The designation of a test that is not required for compliance but is considered important from a characterization standpoint. It is provided for informational purposes only.
Insertion loss	The ratio, expressed in dB, of incident power to delivered power.
Internal cable	A cable that is used to connect a 8639 Initiator Device to a 8639 Target Device within a mainframe.
Near-end crosstalk	Crosstalk that is propagated in a disturbed channel in the opposite direction as the propagation of a signal in the aggressor channel. The terminals of the aggressor channel and the victim channel are usually close to each other.
Normative	The designation of a test that is required for compliance.
Physical link	Two differential signal pairs, one pair in each direction that connect two physical phys (see the current 8639 specification.)
Return Loss	The ratio, expressed in dB, of incident power to reflected power.
8639 Initiator Device	A device containing SSP, STP, and /or SMP initiating ports in a 8639 domain.
8639 Target Device	A device containing SSP, STP, and /or SMP target ports in a 8639 domain.
8639G4-TPA	8639 Gen-4 Test Point Access. A specialized assembly that interfaces to a 8639 Gen-4 receptacle or plug and enables access of signals for measurement or stimulation.
Serial ATA (SATA)	The protocol defined by SATA (see ATA8-AAM)
Serial Attached SCSI (8639G4)	The set of protocols defined in SPL and the interconnect defined by the SFF-8639 Gen-4 specification.
Victim	A signal carrier on a system that has a response imposed on it by other signals in the system.

Addendum A – Testing Specific DUT Configurations

This addendum provides documentation for specific test configurations using the universal SFF-8639 Gen-4 test adapters (PCI Express, SATA Express, and SAS MultiLink) as to content and operation of each.

PCI Express Specific Test Configuration

This section contains illustrations of the universal 8639G4-TPA-P and 8639G4-TPA-R test adapters and the related 8639 Gen-4 Configuration Board used with the 8639G4-TPA-P test adapter when testing PCI Express Specific DUTs.

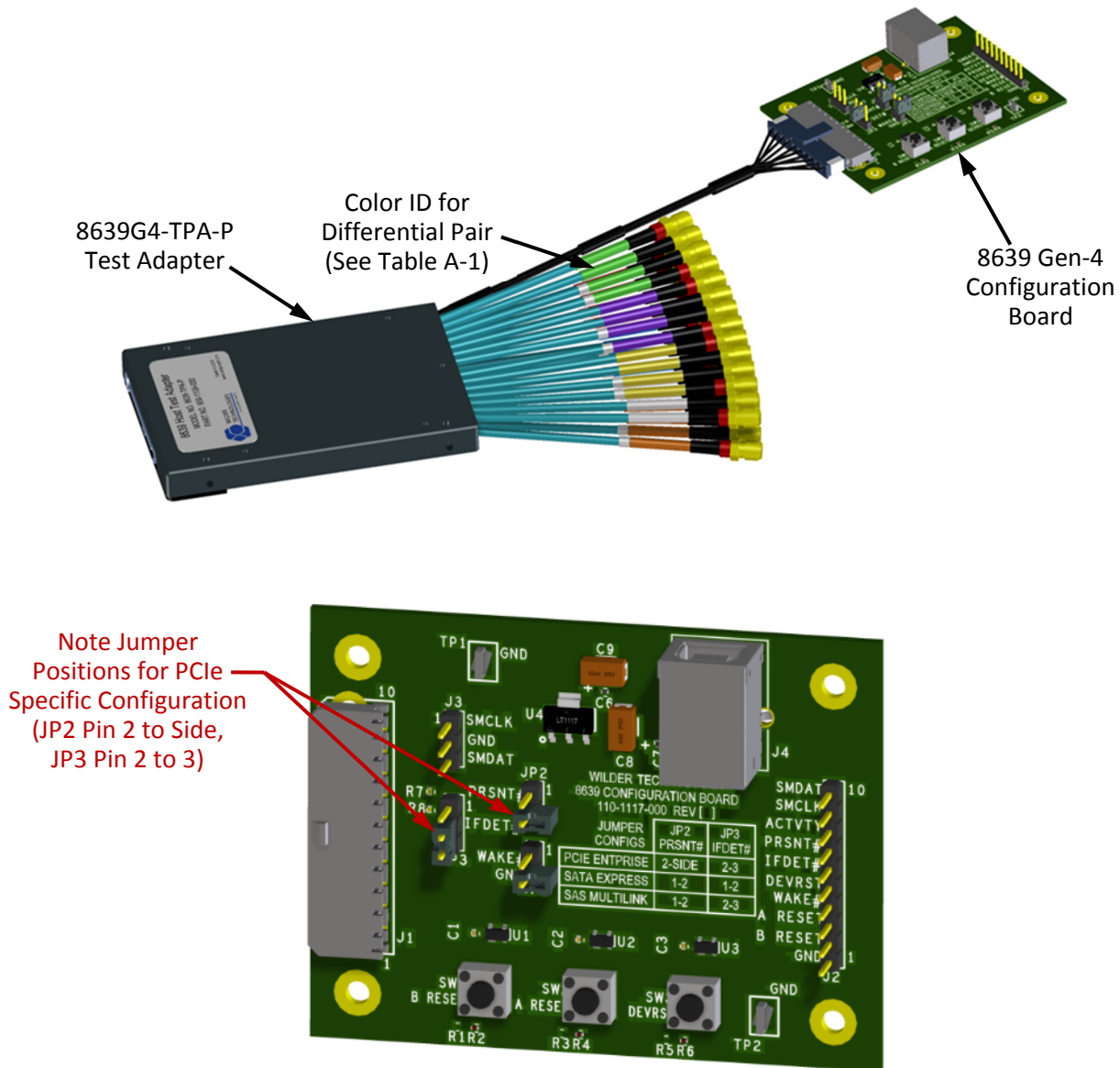


Figure A-1. 8639G4-TPA-P Test Adapter and 8639 Gen-4 Configuration Board

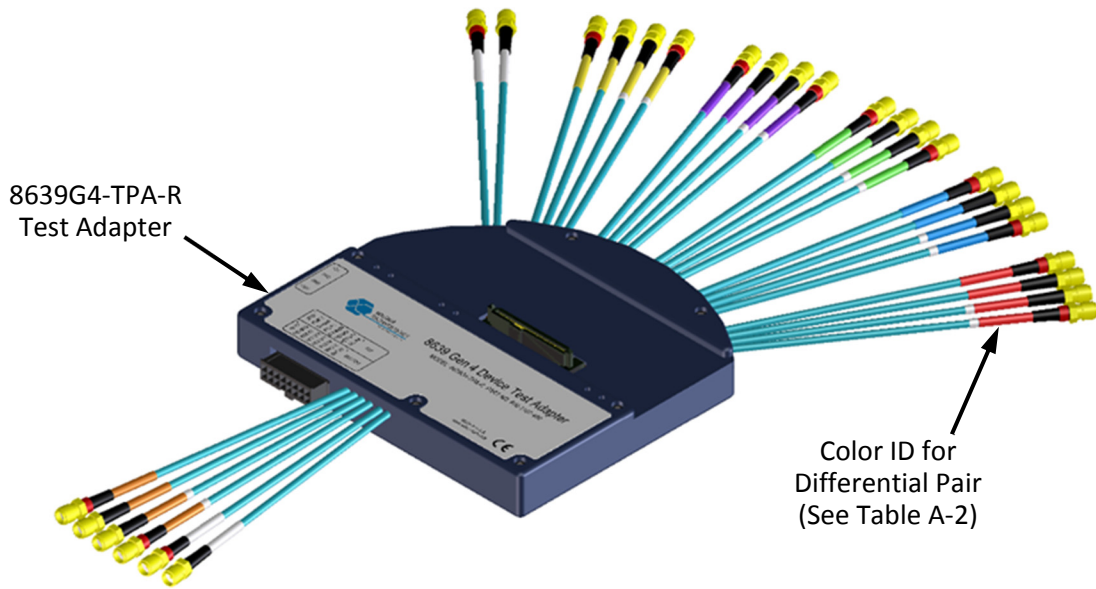


Figure A-2. 8639G4-TPA-R Universal Test Adapter

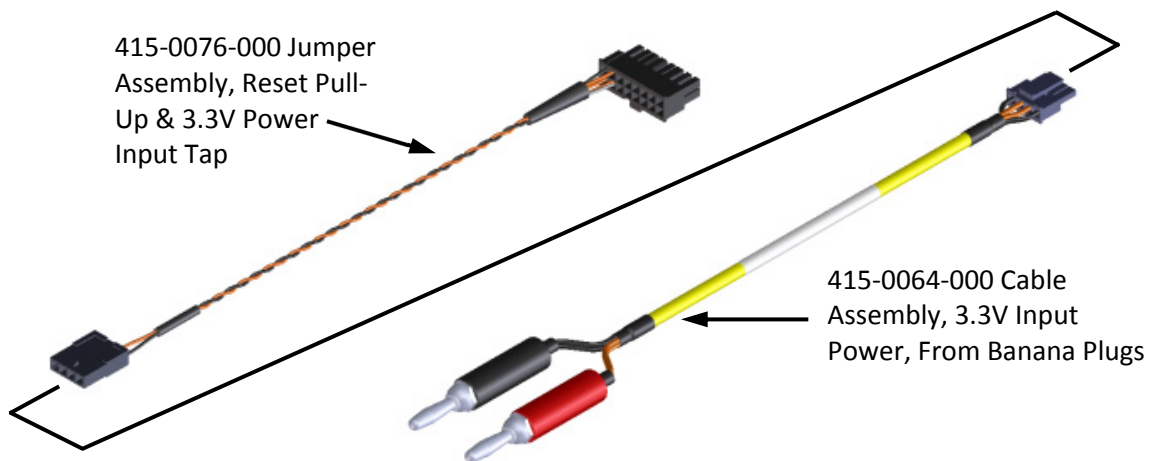


Figure A-3. 8639G4-TPA-R Cable and Jumper Cable Assemblies

The jumper harness assembly (415-0076-000) and the power input cable assembly (415-0064-000) can be used in conjunction to supply 3.3 volts to the TPA and pull-up requirements to PERST and PERSTB. These harness assemblies are provided with the universal receptacle TPA (8639G4-TPA-R).

SATA Express Specific Test Configuration

This section contains illustrations of the universal 8639G4-TPA-P and 8639G4-TPA-R test adapters and the related 8639 Configuration Board used with the 8639G4-TPA-P test adapter when testing SATA Express Specific DUTs.

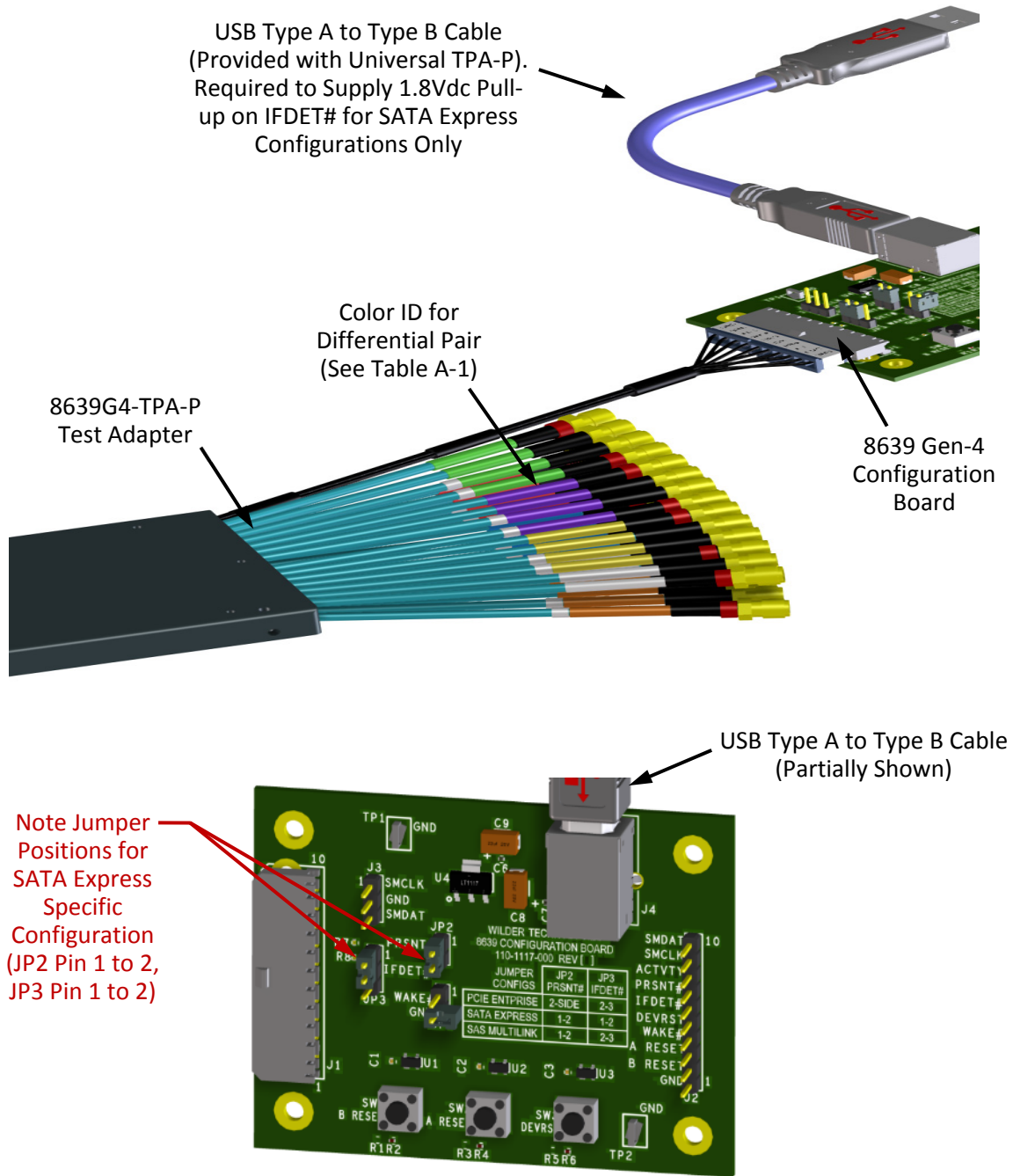


Figure A-4. 8639G4-TPA-P Universal Test Adapter and 8639 Configuration Board

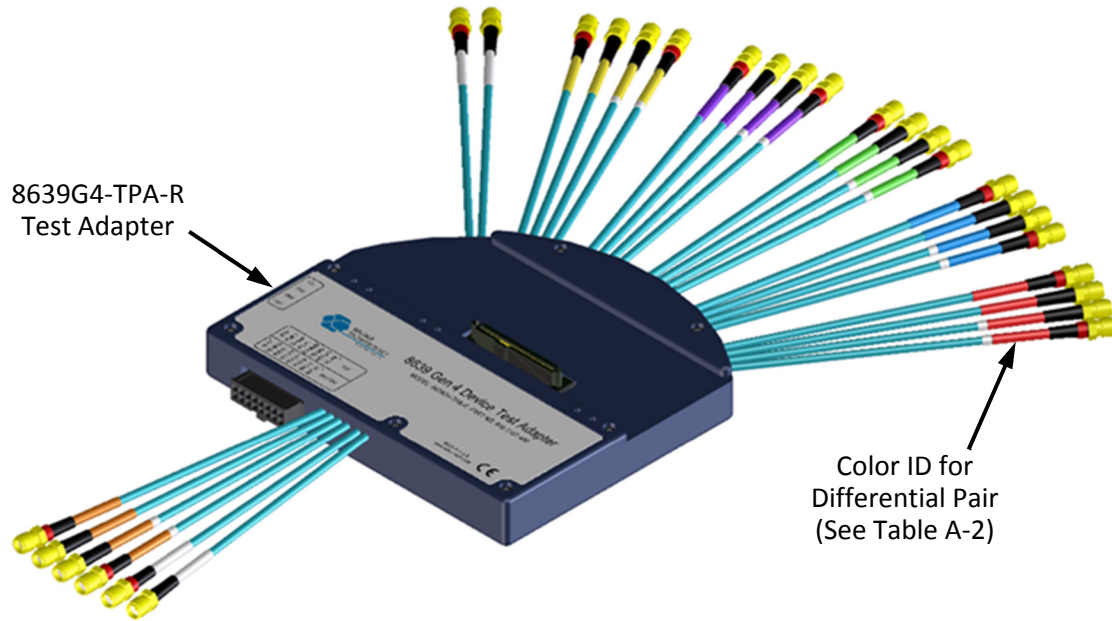


Figure A-5. 8639G4-TPA-R Universal Test Adapter

SAS MultiLink Specific Test Configuration

This section contains illustrations of the universal 8639G4-TPA-P and 8639G4-TPA-R test adapters and the related 8639 Configuration Board used with the 8639G4-TPA-P test adapter when testing SAS MultiLink Specific DUTs.

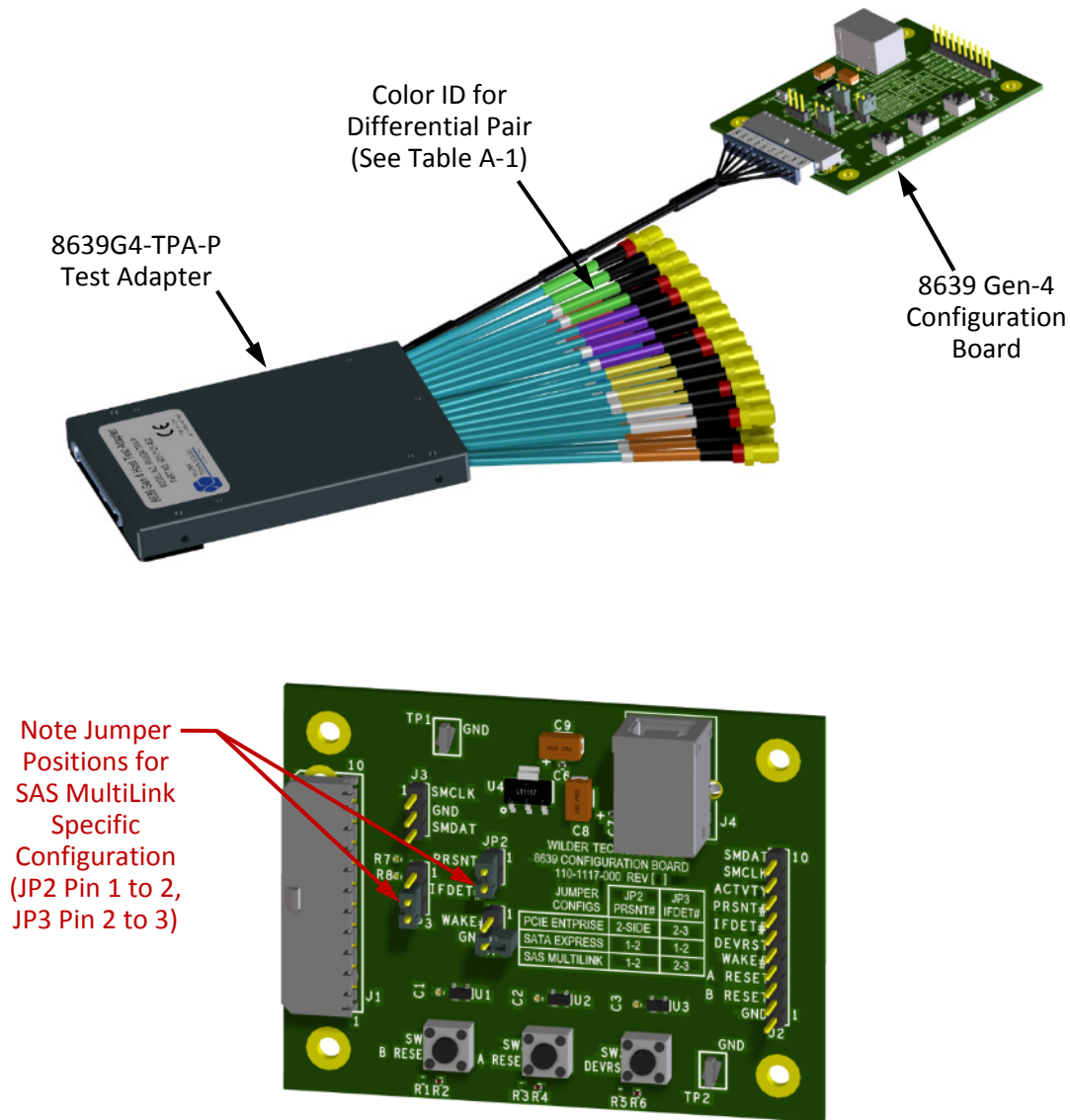


Figure A-6. 8639SX4-TPA-P SAS MultiLink Test Adapter and 8639 Configuration Board

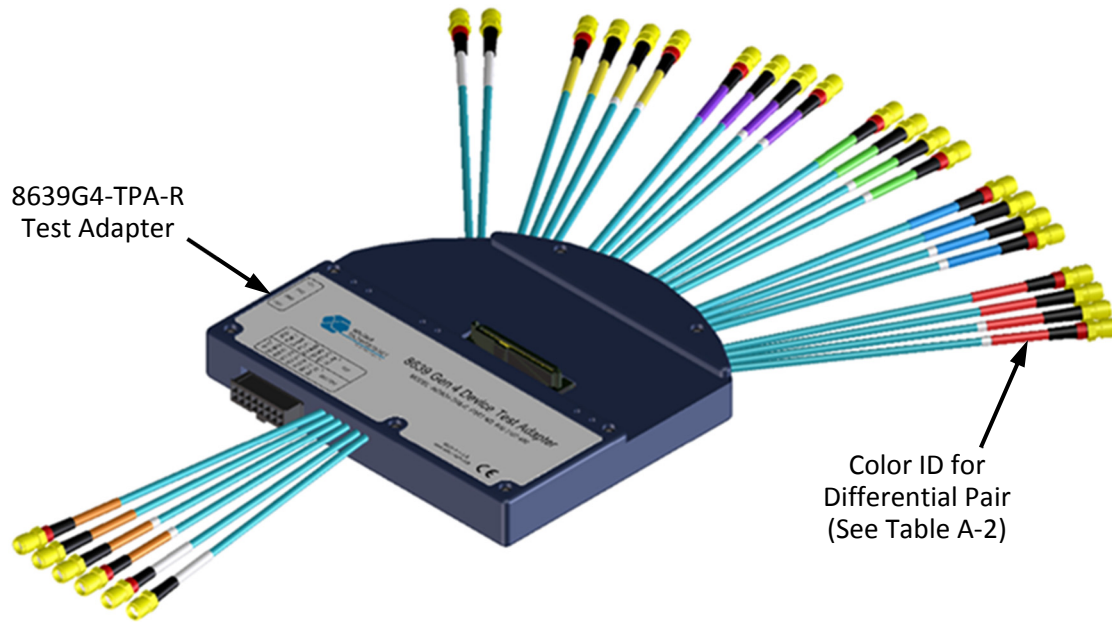


Figure A-7. 8639G4-TPA-R Universal Test Adapter

SFF-8639 Gen-4 Test Adapter User Manual

Table A-1. TPA-P (8639 Specific Configuration Plug) Pin Assignments on keyed side of connector












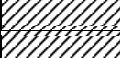

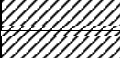





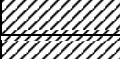





Pin Description	Connector Pin Number	PCI Express 8639. Identification Marker, if Present (Name in Spec.)	SATA Express. Identification Marker, if Present (Name in Spec.)	SAS MultiLink. Identification Marker, if Present (Name in Spec.)	Color Bands (if used)
Signal Ground	S1	Signal Ground, GND	Signal Ground, GND	Signal Ground, GND	
Host SAS/SATA 0 Transmitter Positive	S2	HOST S0T+	HOST S0T+	HOST S0T+	
Host SAS/SATA 0 Transmitter Negative	S3	HOST S0T -	HOST S0T -	HOST S0T -	
Signal Ground	S4	Signal Ground, GND	Signal Ground, GND	Signal Ground, GND	
Host SAS/SATA 0 Receiver Negative	S5	HOST S0R-	HOST S0R-	HOST S0R-	
Host SAS/SATA 0 Receiver Positive	S6	HOST S0R+	HOST S0R+	HOST S0R+	
Signal Ground	S7	Signal Ground, GND	Signal Ground, GND	Signal Ground, GND	
PCIe Ref Clock for Port B Positive	E1	HOST RCLKB+	N/A	N/A	
PCIe Ref Clock for Port B Negative	E2	HOST RCLKB-	N/A	N/A	
+3.3 Volts for SM Bus	E3	0.01 μ F bypass to GND	0.01 μ F bypass to GND	0.01 μ F bypass to GND	
Clock Request/PCIe Reset for Port B	E4	CLKREQ#/PERSTB#	N/A	N/A	
PCIe Reset for Port A	E5	PERST#	N/A	N/A	
Reserved	E6	No Connection	N/A, No Connection	N/A, No Connection	
Device/System Specific Wake-Up	P1	WK# (WAKE#)	WK# (Reserved)	WK# (Pin P1)	
8639 Connector Pin P2	P2	DRS (Pin P2)	DRS (PERST#)	DRS (Pin P2)	
Power Disable or PCIe Reference Clock Request/Device Sleep for SATA Express Only	P3	No Connection	No Connection	No Connection	
Interface Type Detect	P4	ID# (IFDET#)	ID# (IFDET#)	ID# (IFDET#)	
Power Ground	P5, P6	GND	GND	GND	
+5 Volts precharge	P7	N/A, No Connection	No Connection	No Connection	
+5 Volts	P8, P9	N/A, No Connection	No Connection	No Connection	
Device Present	P10	PR# (PRSNT#)	PR# (PRSNT#)	PR# (PRSNT#)	
PCIe Activity	P11	AS (ACTIVITY#)	AS (DAS/DSS)	AS (READY LED)	
Power Ground	P12	GND	GND	GND	
+12 Volts precharge	P13	No Connection	No Connection	No Connection	
+12 Volts	P14, P15	No Connection	No Connection	No Connection	

Table A-1. TPA-P (8639 Specific Configuration Plug) Pin Assignments on side opposed to keyed side of connector





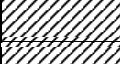



























Pin Description	Connector Pin Number	PCI Express 8639. Identification Marker, if Present (Name in Spec.)	SATA Express. Identification Marker, if Present (Name in Spec.)	SAS MultiLink. Identification Marker, if Present (Name in Spec.)	Color Bands (if used)
PCIe Ref Clock for Port A Positive	E7	HOST RCLKA+	HOST RCLKA+	N/A	
PCIe Ref Clock for Port A Negative	E8	HOST RCLKA-	HOST RCLKA-	N/A	
Signal Ground	E9	Signal Ground, GND	Signal Ground, GND (Doesn't support SRIS)	N/A	
Host PCIe 0 Transmitter Positive	E10	HOST PET0+	N/A	N/A	
Host PCIe 0 Transmitter Negative	E11	HOST PET0-	N/A	N/A	
Signal Ground	E12	Signal Ground, GND	N/A	N/A	
Host PCIe 0 Receiver Negative	E13	HOST PER0-	N/A	N/A	
Host PCIe 0 Receiver Positive	E14	HOST PER0+	N/A	N/A	
Signal Ground	E15	Signal Ground, GND	N/A	N/A	
Reserved	E16	No Connection	N/A	N/A	
Signal Ground	S8	Signal Ground, GND	Signal Ground, GND	Signal Ground, GND	
Host SAS 1 Transmitter Positive	S9	HOST S1T+	HOST S1T+	HOST S1T+	
Host SAS 1 Transmitter Negative	S10	HOST S1T-	HOST S1T-	HOST S1T-	
Signal Ground	S11	Signal Ground, GND	Signal Ground, GND	Signal Ground, GND	
Host SAS 1 Receiver Negative	S12	HOST S1R-	HOST S1R-	HOST S1R-	
Host SAS 1 Receiver Positive	S13	HOST S1R+	HOST S1R+	HOST S1R+	
Signal Ground	S14	Signal Ground, GND	Signal Ground, GND	Signal Ground, GND	
Reserved	S15	No Connection	N/A, No Connection	No Connection	
Signal Ground	S16	Signal Ground, GND	N/A	Signal Ground, GND	
Host PCIe 1 Transmitter Positive	S17	HOST PET1+	N/A	HOST PET1+ (HOST S2T+)	
Host PCIe 1 Transmitter Negative	S18	HOST PET1-	N/A	HOST PET1- (HOST S2T-)	
Signal Ground	S19	Signal Ground, GND	N/A	Signal Ground, GND	
Host PCIe 1 Receiver Negative	S20	HOST PER1-	N/A	HOST PER1- (HOST S2R-)	
Host PCIe 1 Receiver Positive	S21	HOST PER1+	N/A	HOST PER1+ (HOST S2R+)	
Signal Ground	S22	Signal Ground, GND	N/A	Signal Ground, GND	

Table A-1. TPA-P (8639 Specific Configuration Plug) Pin Assignments on side opposed to keyed side of connector (continued)

Pin Description	Connector Pin Number	PCI Express 8639. Identification Marker, if Present (Name in Spec.)	SATA Express. Identification Marker, if Present (Name in Spec.)	SAS MultiLink. Identification Marker, if Present (Name in Spec.)	Color Bands (if used)
Host PCIe 2 Transmitter Positive	S23	HOST PET2+	N/A	HOST PET2+ (HOST S3T+)	
Host PCIe 2 Transmitter Negative	S24	HOST PET2-	N/A	HOST PET2- (HOST S3T-)	
Signal Ground	S25	Signal Ground, GND	N/A	Signal Ground, GND	
Host PCIe 2 Receiver Negative	S26	HOST PER2-	N/A	HOST PER2- (HOST S3R-)	
Host PCIe 2 Receiver Positive	S27	HOST PER2+	N/A	HOST PER2+ (HOST S3R+)	
Signal Ground	S28	Signal Ground, GND	N/A	Signal Ground, GND	
Host PCIe 3 Transmitter Positive	E17	HOST PET3+	N/A	N/A	
Host PCIe 3 Transmitter Negative	E18	HOST PET3-	N/A	N/A	
Signal Ground	E19	Signal Ground, GND	N/A	N/A	
Host PCIe 3 Receiver Negative	E20	HOST PER3-	N/A	N/A	
Host PCIe 3 Receiver Positive	E21	HOST PER3+	N/A	N/A	
Signal Ground	E22	Signal Ground, GND	N/A	N/A	
SM-Bus Clock	E23	SMC (SMCLK)	N/A	N/A	
SM-Bus Data	E24	SMD (SMDAT)	N/A	N/A	
PCIe Dual Link Enable	E25	No connection (DualLinkEn#)	N/A	N/A	

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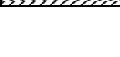
Table A-2. TPA-R (8639 Specific Configuration Receptacle) Pin Assignments on keyed side of connector

Pin Description	Connector Pin Number	PCI Express 8639. Identification Marker, if Present (Name in Spec.)	SATA Express. Identification Marker, if Present (Name in Spec.)	SAS MultiLink. Identification Marker, if Present (Name in Spec.)	Color Bands (if used)
Signal Ground	S1	Signal Ground, GND	Signal Ground, GND	Signal Ground, GND	
Device SAS/SATA 0 Receiver Positive	S2	DEV S0R+	DEV S0R+	DEV S0R+	
Device SAS/SATA 0 Receiver Negative	S3	DEV S0R -	DEV S0R -	DEV S0R -	
Signal Ground	S4	Signal Ground, GND	Signal Ground, GND	Signal Ground, GND	
Device SAS/SATA 0 Transmitter Negative	S5	DEV S0T-	DEV S0T-	DEV S0T-	
Device SAS/SATA 0 Transmitter Positive	S6	DEV S0T+	DEV S0T+	DEV S0T+	
Signal Ground	S7	Signal Ground, GND	Signal Ground, GND	Signal Ground, GND	
PCIe Ref Clock for Port B Positive	E1	DEV RCLKB+	N/A	N/A	
PCIe Ref Clock for Port B Negative	E2	DEV RCLKB-	N/A	N/A	
+3.3 Volts for SM Bus	E3	+3.3V	N/A, +3.3V	N/A, +3.3V	
Clock Request/PCIe Reset for Port B	E4	PIN E4 (CLKREQ#/PERSTB#)	N/A, PIN E4	N/A, PIN E4	
PCIe Reset for Port A	E5	PERST#	N/A, PIN E5	N/A, PIN E5	
Reserved	E6	RES E6	N/A, PIN E6	N/A, PIN E6	
Device/System Specific Wake-Up	P1	WAKE#	WAKE# (RES P1 Reserved)	WAKE# (PIN P1 Vendor Specific)	
8639 Connector Pin P2	P2	N/A, PIN P2	N/A, PIN P2 (PERST#)	PIN P2 (PIN P2 Vendor Specific)	
Power Disable or PCIe Reference Clock Request/Device Sleep for SATA Express Only	P3	PIN P3 (PWRDIS)	PIN P3 (CLKREQ#/DEVSLP)	PIN P3 (PWRDIS)	
Interface Type Detect	P4	IFDET#	IFDET#	IFDET#	
Power Ground	P5, P6	GND	GND	GND	
+5 Volts precharge	P7	N/A, +5V 2 Ohm Resistor to +5V	N/A, +5V 2 Ohm Resistor to +5V	N/A, +5V 2 Ohm Resistor to +5V	
+5 Volts	P8, P9	N/A, +5V	N/A, +5V	N/A, +5V	
Device Present	P10	PRSNT#	PRSNT#	PRSNT#	
PCIe Activity	P11	ACTIVITY# (ACTIVITY#)	ACTIVITY# (DAS/DSS)	ACTIVITY# (READY LED)	
Power Ground	P12	GND	GND	GND	
+12 Volts precharge	P13	+12V, 2 Ohm Resistor to +12V	+12V, 2 Ohm Resistor to +12V	+12V, 2 Ohm Resistor to +12V	
+12 Volts	P14, P15	+12V	+12V	+12V	

Table A-2. TPA-R (8639 Specific Configuration Receptacle) Pin Assignments on side opposed to keyed side of connector

Pin Description	Connector Pin Number	PCI Express 8639. Identification Marker, if Present (Name in Spec.)	SATA Express. Identification Marker, if Present (Name in Spec.)	SAS MultiLink. Identification Marker, if Present (Name in Spec.)	Color Bands (if used)
PCIe Ref Clock for Port A Positive	E7	DEV RCLKA+	DEV RCLKA+	N/A	
PCIe Ref Clock for Port A Negative	E8	DEV RCLKA-	DEV RCLKA-	N/A	
Signal Ground	E9	Signal Ground, GND	Signal Ground, GND (Doesn't support SRIS)	N/A	
Device PCIe 0 Receiver Positive	E10	DEV PER0+	N/A	N/A	
Device PCIe 0 Receiver Negative	E11	DEV PER0-	N/A	N/A	
Signal Ground	E12	Signal Ground, GND	N/A	N/A	
Device PCIe 0 Transmitter Negative	E13	DEV PET0-	N/A	N/A	
Device PCIe 0 Transmitter Positive	E14	DEV PET0+	N/A	N/A	
Signal Ground	E15	Signal Ground, GND	N/A	N/A	
Reserved	E16	PIN E16 (Reserved)	N/A, PIN E16	N/A, PIN E16	
Signal Ground	S8	Signal Ground, GND	Signal Ground, GND	Signal Ground, GND	
Device SAS 1 Receiver Positive	S9	DEV S1R+	DEV S1R+	DEV S1R+	
Device SAS 1 Receiver Negative	S10	DEV S1R-	DEV S1R-	DEV S1R-	
Signal Ground	S11	Signal Ground, GND	Signal Ground, GND	Signal Ground, GND	
Device SAS 1 Transmitter Negative	S12	DEV S1T-	DEV S1T-	DEV S1T-	
Device SAS 1 Transmitter Positive	S13	DEV S1T+	DEV S1T+	DEV S1T+	
Signal Ground	S14	Signal Ground, GND	Signal Ground, GND	Signal Ground, GND	
Reserved	S15	PIN S15 (Reserved)	N/A, PIN S15	PIN S15 (Reserved)	
Signal Ground	S16	Signal Ground, GND	N/A	Signal Ground, GND	
Device PCIe 1 Receiver Positive	S17	DEV PER1+	N/A	DEV PER1+ (DEV S2R+)	
Device PCIe 1 Receiver Negative	S18	DEV PER1-	N/A	DEV PER1- (DEV S2R-)	
Signal Ground	S19	Signal Ground, GND	N/A	Signal Ground, GND	
Device PCIe 1 Transmitter Negative	S20	DEV PET1-	N/A	DEV PET1- (DEV S2T-)	
Device PCIe 1 Transmitter Positive	S21	DEV PET1+	N/A	DEV PET1+ (DEV S2T+)	
Signal Ground	S22	Signal Ground, GND	N/A	Signal Ground, GND	

Table A-2. TPA-R (8639 Specific Configuration Receptacle) Pin Assignments on side opposed to keyed side of connector (continued)

Pin Description	Connector Pin Number	PCI Express 8639. Identification Marker, if Present (Name in Spec.)	SATA Express. Identification Marker, if Present (Name in Spec.)	SAS MultiLink. Identification Marker, if Present (Name in Spec.)	Color Bands (if used)
Device PCIe 2 Receiver Positive	S23	DEV PER2+	N/A	DEV PER2+ (DEV S3R+)	
Device PCIe 2 Receiver Negative	S24	DEV PER2-	N/A	DEV PER2- (DEV S3R-)	
Signal Ground	S25	Signal Ground, GND	N/A	Signal Ground, GND	
Device PCIe 2 Transmitter Negative	S26	DEV PET2-	N/A	DEV PET2- (DEV S3T-)	
Device PCIe 2 Transmitter Positive	S27	DEV PET2+	N/A	DEV PET2+ (DEV S3T+)	
Signal Ground	S28	Signal Ground, GND	N/A	Signal Ground, GND	
Device PCIe 3 Receiver Positive	E17	DEV PER3+	N/A	N/A	
Device PCIe 3 Receiver Negative	E18	DEV PER3-	N/A	N/A	
Signal Ground	E19	Signal Ground, GND	N/A	N/A	
Device PCIe 3 Transmitter Negative	E20	DEV PET3-	N/A	N/A	
Device PCIe 3 Transmitter Positive	E21	DEV PET3+	N/A	N/A	
Signal Ground	E22	Signal Ground, GND	N/A	N/A	
SM-Bus Clock	E23	SMC (SMCLK)	N/A, PIN E23	N/A, PIN E23	
SM-Bus Data	E24	SMD (SMDAT)	N/A, PIN E24	N/A, PIN E24	
PCIe Dual Link Enable	E25	No connection (DualLinkEn#)	N/A, PIN E25	N/A, PIN E25	

Addendum B – 8639 Configuration Board Reference Information

This addendum provides reference information for the 8639 Configuration Board with regard to the SFF-8639 test adapters (PCI Express, SATA Express, and SAS MultiLink). Additional details of the 8639 Gen-4 Configuration Board itself are also presented.

8639 Configuration Board Jumper Positions

The following illustration depicts the 8639 Gen-4 Configuration Board in the “as delivered” product, with all jumpers positioned to the “Neutral/Park” positions. The table that follows depicts the jumper positions for each of the specific interface types (PCI Express 8639, SATA Express, and SAS MultiLink) that are required to have the device recognized by the system.

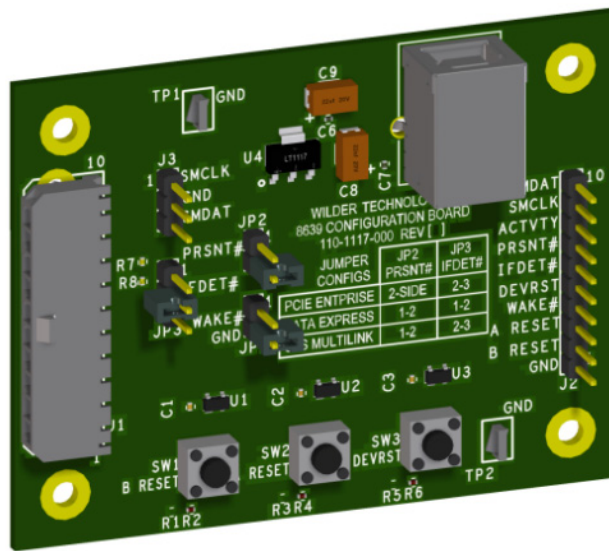
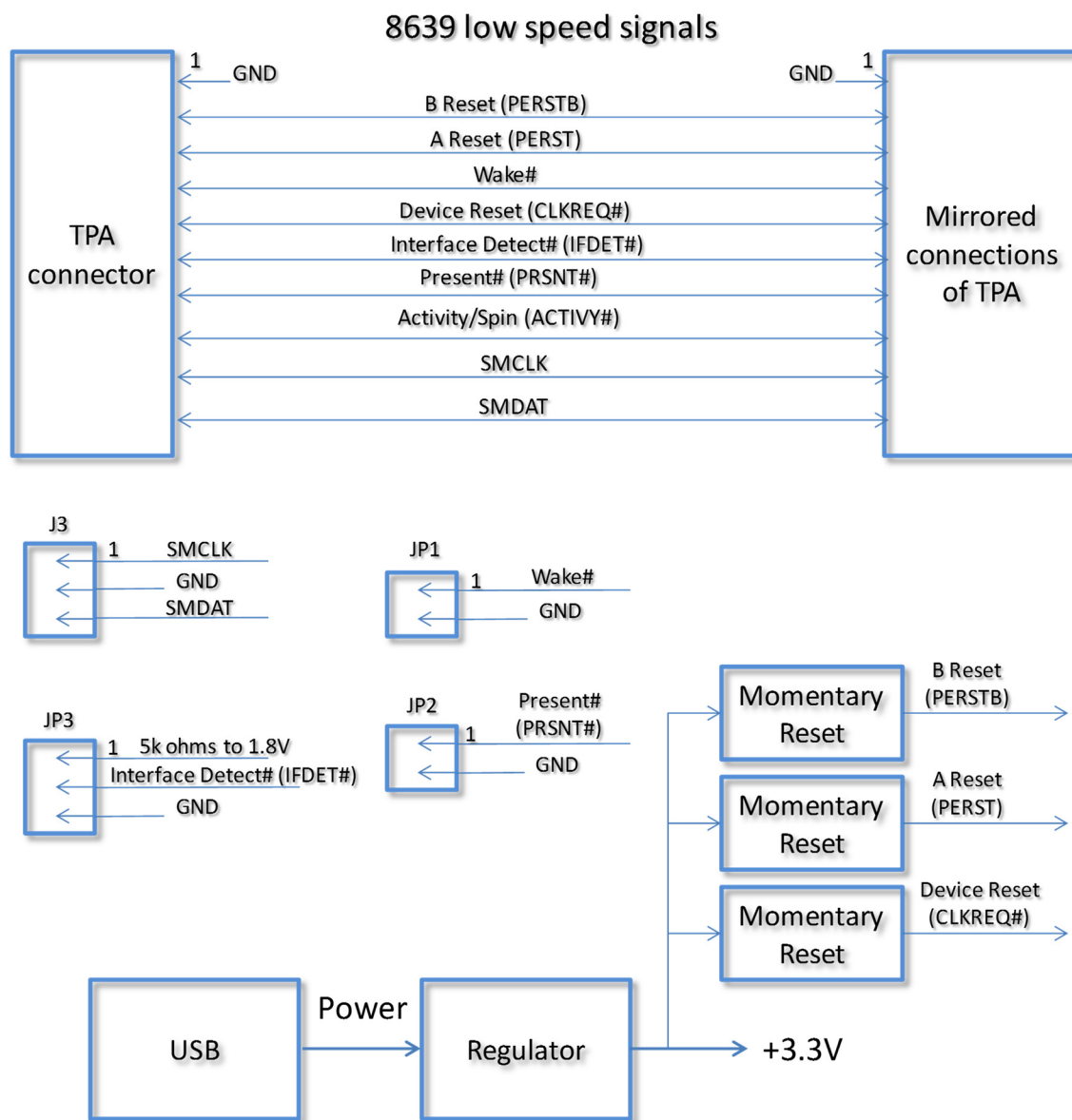


Figure B-1. 8639 Gen-4 Configuration Board

Table B-1. 8639 Configuration Board Jumper Positions

JUMPER CONFIGURATIONS	JP2 (PRSNT#)	JP3 (IFDET#)	COMMENT
PCIe 8639 (Enterprise)	Pin 2 to Side (Open/Park)	Pin 2 to Pin 3 (Ground)	
SATA Express	Pin 1 to Pin 2 (Ground)	Pin 1 to Pin 2 (Pulled-up to 1.8 Vdc)	Requires USB Cable and Connection
SAS MultiLink	Pin 1 to Pin 2 (Ground)	Pin 2 to Pin 3 (Ground)	
No Device Present	Pin 2 to Side (Open/Park)	Pin 2 to Side (Open/Park)	

8639 Configuration Board Block Diagram



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