

# PCIe M.2 Socket 2 Test Adapter

User Manual



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### Introduction

This user's guide documents the PCIe M.2 Socket 2 Host and Device Test Adapters (PCIeM2-TPA2-P and PCIeM2-TPA2-R, respectively). The two test adapter types, shown in Figures 1 and 2, test PCIe M.2 Socket 2 hosts and devices against the PCIe M.2 Specification.

The TPA-P and TPA-R test adapter assemblies allow easy access, via SMA connections, to measure or inject data signals. The Receptacle test adapter also provides access to +3.3V, and their respective GNDs, via a 4-position power connector. Additionally, a 14-position low-speed connector is provided for access to commonly used low-speed signals. For less-commonly used low-speed signals, an array of 26 pins (.025 square posts) and an array of 8 pins (.025 square posts) are also provided for user access. Mating 4-position power cables and 14-position connector housing and contacts are provided to connect the above power and/or a low speed wiring assembly. Mating connectors are not supplied for the 26-position and 8-position connector pin/post arrays.

**NOTE: To avoid damaging the cables, use the handling techniques described in the Care and Handling section before making any connections or configuring a test setup.**

**Always use a static-safe workstation when performing tests, as explained in the "Electrostatic Discharge Information" section.**

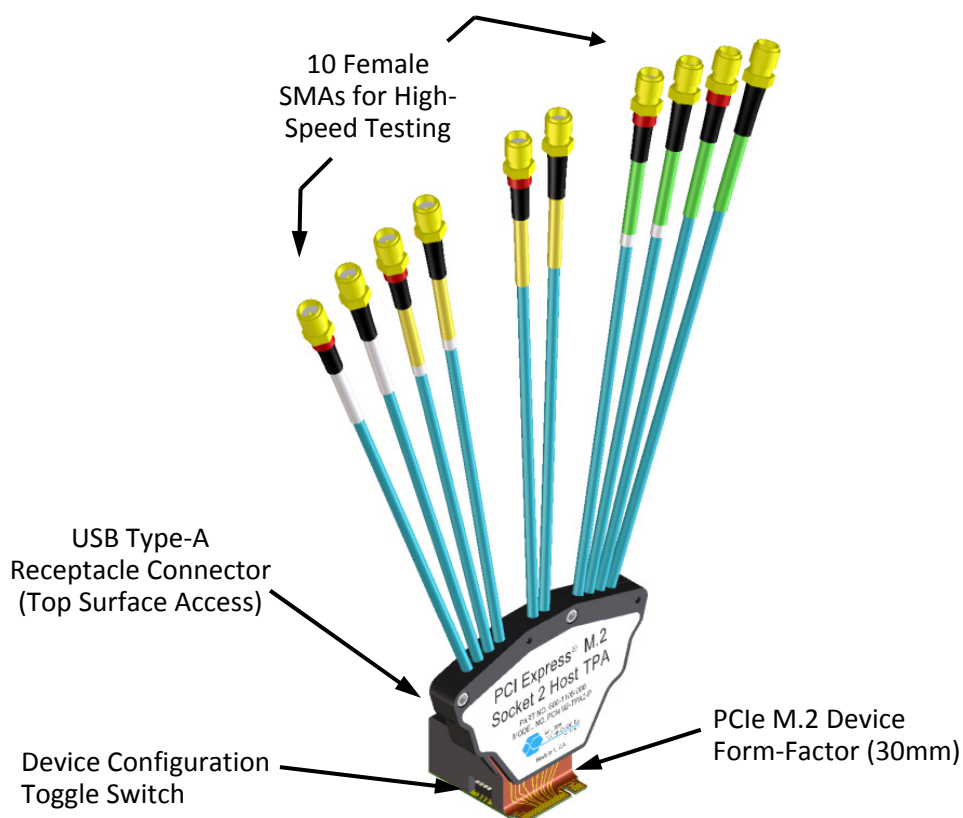


Figure 1. The PCIe M.2 Socket 2 Host Test Adapter (Plug)

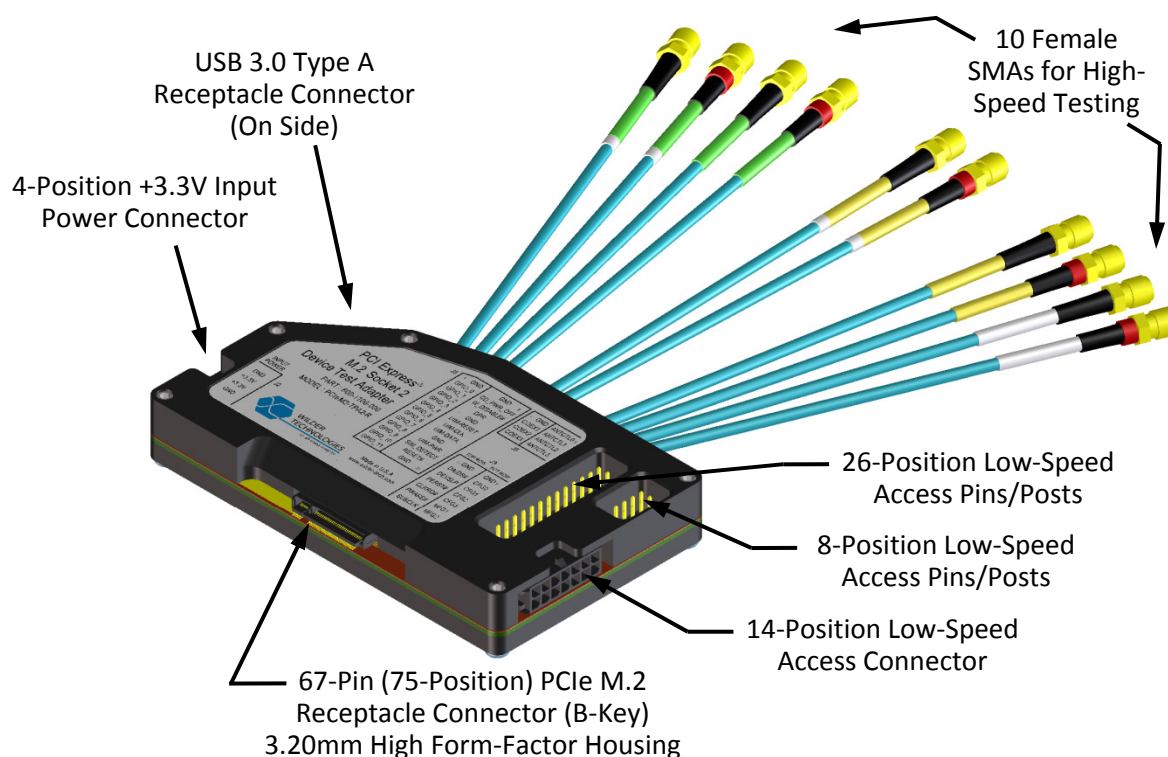


Figure 2. The PCIe M.2 Socket 2 Device Test Adapter (Receptacle)

The 4-position input power connector used in the receptacle test adapter is Molex part number 43650-0404 and is used with one of the two versions of input power cable assemblies, provided with each PCIe M.2-TPA2-R.

The 14-position low-speed connector is Molex part number 43045-1402. A mating 14-position receptacle connector housing and contact pins for 26-30awg wire are provided with each PCIe M.2-TPA2-R assembly (Molex part number 43025-1400 for the 14-position low-speed connector housing, and 43030-0011 for the 26-30awg pin contacts). Replacement receptacle housings or contacts can be purchased through Molex distributors.

NOTE: Mating connector housings and contacts are not supplied for either the 26-position or the 8-position low-speed access pins/posts.

## Product Inspection

Upon receiving the PCIeM2-TPA2 from Wilder Technologies, perform the following product inspection:

- Inspect the outer shipping container, foam-lined instrument case, and product for damage. Retain the outer cardboard shipping container until the contents of the shipment have been inspected for completeness and the product has been checked mechanically and electrically. Use the foam-lined instrument-case for secure storage of the Wilder Technologies PCIe M.2 Socket 2 Test Adapter when not in use.
- Locate the shipping list and verify that all items ordered were received.
- In the unlikely event that the product is defective or incomplete, the “Limited Warranty” section discusses how to contact Wilder Technologies for technical assistance and/or how to package the product for return.

## The PCIe M.2 Socket 2 Test Adapter Care and Handling Precautions

The PCIe M.2 Socket 2 Test Adapter requires careful handling to avoid damage. Improper handling techniques, or using too small a cable bend radius, can damage the coaxial cable connections within the adapter housing or the cables themselves. This can occur at any point along the cable. To achieve optimum performance and to prolong the PCIeM2-TPA2's life, observe the following handling precautions:

- **CAUTION 1: Avoid Torque Forces (Twisting)**  
While individual coaxial cables within the test adapter have some rotational freedom, twisting the PCIeM2-TPA2 as a unit, with one end held stationary, may damage or severely degrade performance. Adherence to Caution 5 (below) helps to avoid twisting.
- **CAUTION 2: Avoid Sharp Cable Bends**  
Never bend coaxial cables into a radius of 26 mm (1-inch) or less. Never bend cables greater than 90°. Single or multiple cable bends must be kept within this limit. Bending the PCIeM2-TPA2 cables less than a 26mm (1-Inch) radius will permanently damage or severely degrade test adapter performance.
- **CAUTION 3: Avoid Cable Tension (Pull Forces)**  
Never apply tension (pull forces) to an individual coaxial cable that is greater than 2.3 kg (5 lbs.). To avoid applying tension, always place accessories and equipment on a surface that allows adjustment to eliminate tension on the PCIeM2-TPA2 and cables. Use adjustable elevation stands or apparatus to accurately place and support the PCIeM2-TPA2.
- **CAUTION 4: Connect the PCIeM2-TPA2 First**  
To prevent twisting, bending, or applying tension to the coaxial cables when connecting a PCIeM2-TPA2, always attach the PCIeM2-TPA2 to the device under test (DUT) or cable under test before attaching any SMA connectors. Carefully align the PCIe M.2 connectors and then gently push the connectors together until fully seated (see also Caution 7).

If the PCIeM2-TPA2 must be turned or twisted to make connection to the DUT, avoid using the PCIeM2-TPA2 housing alone to make this occur. Try to distribute the torque forces along the length of the test setup and cabling. If this is not possible, it is recommended to first loosen or disconnect the SMA connections at the PCIeM2-TPA2, make the connection to the DUT and then re-tighten or attach the test equipment leads.

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**NOTE: Only grip the test adapter housing when inserting or extracting the PCIeM2-TPA2 to or from the DUT. Pulling directly on the PCIeM2-TPA2 cables or using them to insert the PCIeM2-TPA2 may cause damage.**

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- **CAUTION 5: Carefully Make SMA Connections**

To connect the PCIeM2-TPA2 SMA connectors, follow these steps:

1. Hold the cable stationary by grasping the cable at the black heat-shrink section near the SMA connector.
2. Insert the mating SMA barrel and hand-tighten the free-spinning SMA nut onto the connector while avoiding pulling, bending, or twisting the PCIeM2-TPA2 coaxial cable.
3. The PCIeM2-TPA2 SMA connectors have flats that accept an open-end 1/4-inch or 6.5mm wrench. When attaching instrument cables to the PCIeM2-TPA2, it is recommended that the PCIeM2-TPA2 SMA connectors be mechanically held and the test leads be tightened to the equipment manufacturer's torque recommendations, normally 5 in-lbs, using a 5/16-inch open-end wrench.

If the test set-up requires repositioning, first loosen or disconnect the SMA connections to avoid twisting, bending, or tension.

---

**NOTE: A drop in signal amplitude by half or 6db during the testing of a channel may indicate that a cable has been mechanically pulled free of coaxial cable connections internal to the assembly. This could be determined by checking if the cable has any lateral play relative to the TPA. This would only occur when the TPA has exceeded the pull force as specified within the mechanical specification. If the cable cannot be re-seated, the test adapter will need to be sent back to the factory for service.**

---

- **CAUTION 6: Independently Support Instrument Cables or Accessories**

Excessive weight from instrument cables and/or accessories connected to the PCIeM2-TPA2 can cause damage or affect the test adapter performance. Be sure to provide appropriate means to support and stabilize all test set-up components.

- **CAUTION 7: Observe M.2 (NGFF) Mini-Card Module Insertion/Removal Instructions**

Users that are unfamiliar with the M.2 (NGFF) connector interface and the associated module (device or TPA) insertion and removal process are encouraged to review Tyco Electronics document 114-115006, Section 3.13 for guidance (see link, below and the extracted guideline section on the following page). *(Courtesy of TE Connectivity)*

[http://www.te.com/commerce/DocumentDelivery/DDEController?Action=showdoc&DocId=Specification+Or+Standard%7F114-115006%7FA%7Fpdf%7FEnglish%7FENG\\_SS\\_114-115006\\_A.pdf%7FN-A](http://www.te.com/commerce/DocumentDelivery/DDEController?Action=showdoc&DocId=Specification+Or+Standard%7F114-115006%7FA%7Fpdf%7FEnglish%7FENG_SS_114-115006_A.pdf%7FN-A)

- **CAUTION 7 (Continued): M.2 (NGFF) Mini-Card Module Insertion/Removal Instructions**  
Extracted from Tyco Electronics Application Note 114-115006 (Courtesy of TE Connectivity).

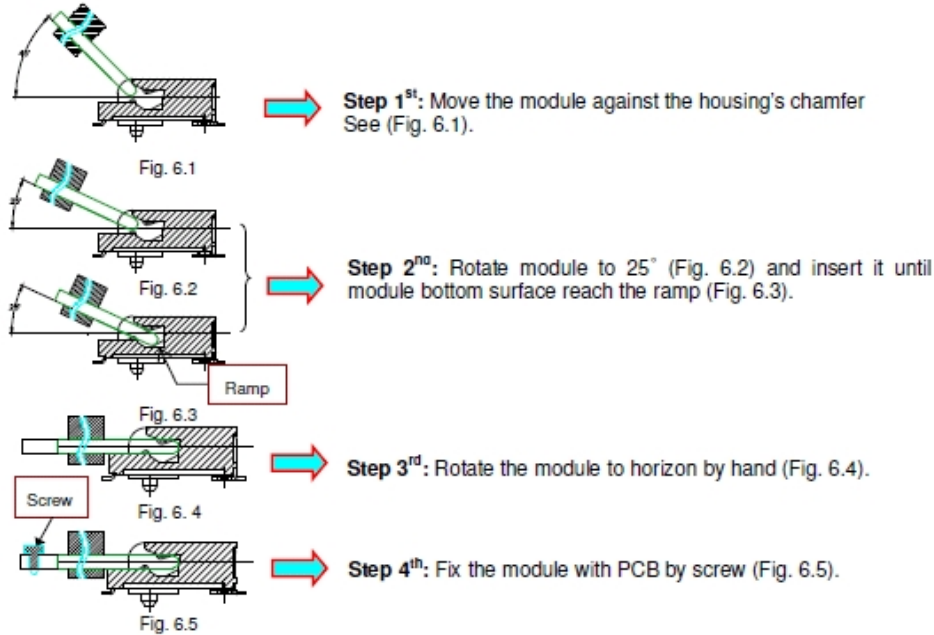


67 Positions 0.5 Pitch M.2(NGFF) MINICARD

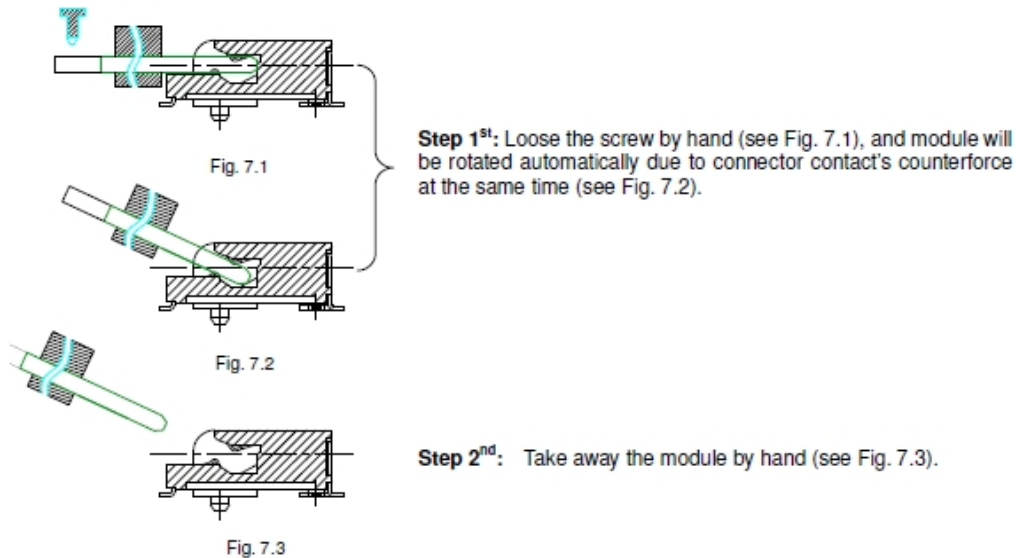
114-115006

### 3.13. Module Insertion and Removal Process

#### A. Module Insertion Process for 2.25H, 3.2H, and 4.2H



#### B. Module Removal Process for 2.25H, 3.2H, and 4.2H





## General Test Adapter, Cable, and Connector

Observing simple precautions can ensure accurate and reliable measurements.

### Handling and Storage

Before each use of the PCIeM2-TPA2, ensure that all connectors are clean. Handle all cables carefully and store the PCIeM2-TPA2 in the foam-lined instrument case when not in use, if possible. Do not set connectors contact end down. Install the SMA protective end caps when the PCIeM2-TPA2 is not in use.

### Visual Inspection

Be sure to inspect all cables carefully before making a connection. Inspect all cables for metal particles, scratches, deformed threads, dents, or bent, broken, or misaligned center conductors. Do not use damaged cables.

### Cleaning

If necessary, clean the connectors using low-pressure (less than 60 PSI) compressed air or nitrogen with an effective oil-vapor filter and condensation trap. Clean the cable threads, if necessary, using a lint-free swab or cleaning cloth moistened with isopropyl alcohol. Always completely dry a connector before use. Do not use abrasives to clean the connectors. Re-inspect connectors, making sure no particles or residue remains.

### Making Connections

Before making any connections, review the “Care and Handling Precautions” section. Follow these guidelines when making connections:

- Align cables carefully
- Make preliminary connection lightly
- To tighten, turn connector nut only
- Do not apply bending force to cable
- Do not over-tighten preliminary connections
- Do not twist or screw-in cables
- Use an appropriately sized torque wrench (depends on SMA gender), and do not tighten past the “break” point of the torque wrench (normally set to 5 in-lbs)

## Electrostatic Discharge Information

Protection against electrostatic discharge (ESD) is essential while connecting, inspecting, or cleaning the PCIeM2-TPA2 test adapter and connectors attached to a static-sensitive circuit (such as those found in test sets).

Electrostatic discharge can damage or destroy electronic components. Be sure to perform all work on electronic assemblies at a static-safe work station, using two types of ESD protection:

- Conductive table-mat and wrist-strap combination
- Conductive floor-mat and heel-strap combination

When used together, both of these types provide a significant level of ESD protection. Used alone, the table-mat and wrist-strap combination provide adequate ESD protection. To ensure user safety, the static-safe accessories must provide at least 1 M $\Omega$  of isolation from ground. Acceptable ESD accessories may be purchased from a local supplier.

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**WARNING: These techniques for a static-safe work station should not be used when working on circuitry with a voltage potential greater than 500 volts.**

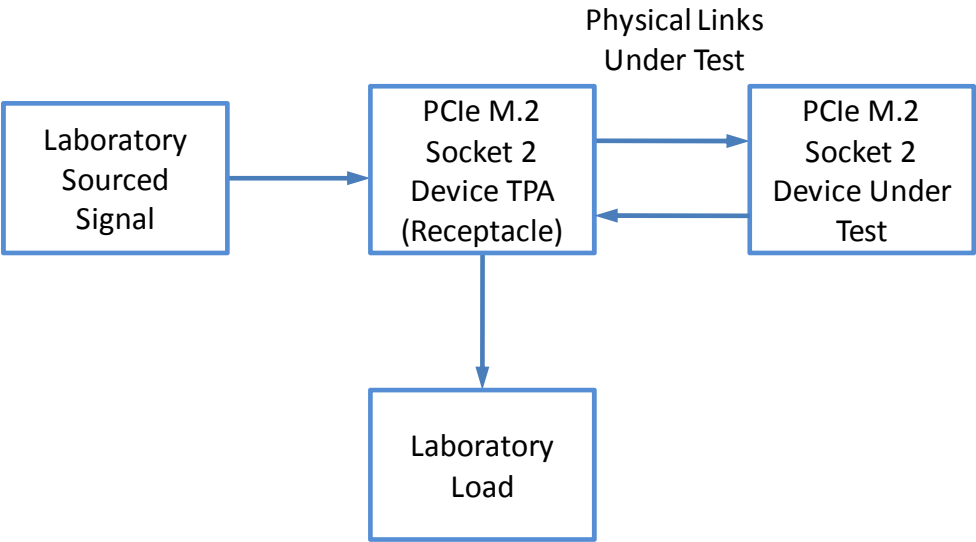
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## User Model

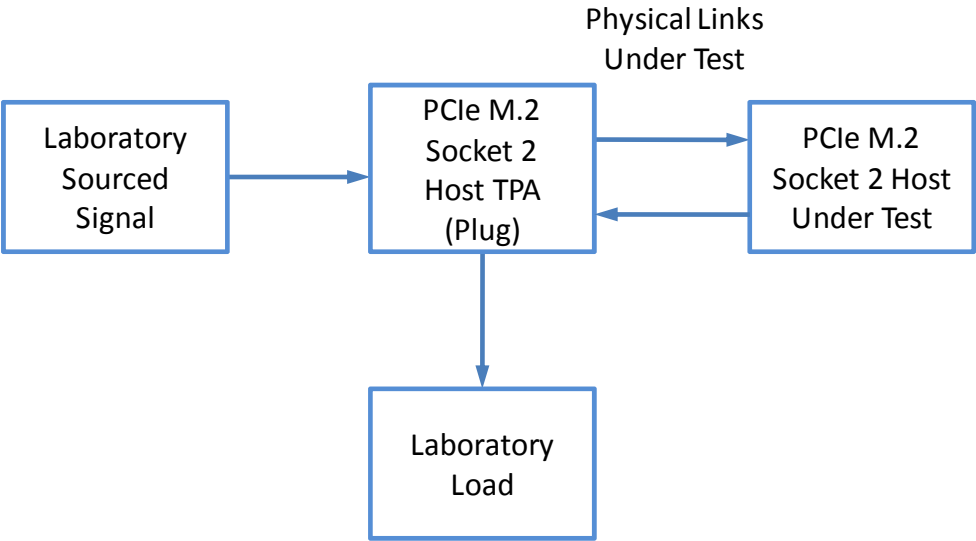
The PCIeM2-TPA2 supports all testing of the PCIe M.2 Specification. It is capable of performing well beyond the scope of measurements required, limited only by the specifications, environmental, care and handling as stated in this document.

The following examples are suggestions for possible testing setups.

In this first example, a PCIe M.2 Socket 2 Device (Receptacle) TPA is used to test a PCIe M.2 Socket 2 device:



The second example shows a PCIe M.2 Socket 2 Host (Plug) TPA used to test a host:



## Calibration Through De-Embedding

The PCIe M.2 Socket 2 Host and Device Test Adapters are fully passive components. Therefore, calibration compensating for the losses must occur within the test instrumentation that drives the PCIe M.2 receiver or looks at the response of the PCIe M.2 transmitter.

The PCIeM2-TPA2's have Touchstone S4P files for de-embedding the electrical length and losses within the TPA up to the PCIe M.2 connector interface pads. (Contact Wilder Technologies, [support@wilder-tech.com](mailto:support@wilder-tech.com), to obtain a copy of the S4P files.) The Touchstone S4P files enable the test engineer to compensate for the last four of the following six repeatable, systematic errors that occur when moving the reference plane:

- Signal leakage effects: *Directivity errors*
- Signal leakage effects: *Crosstalk errors*
- Reflection effects: *Source Impedance Mismatching errors*
- Reflection effects: *Load Impedance Mismatching errors*
- Bandwidth effects: *Receiver Transmission in Test Equipment errors*
- Bandwidth effects: *Receiver Reflection-tracking in Test Equipment errors*

These errors are corrected on each port. Refer to the Instrument Manual for instructions on the instrument's specific de-embedding process.

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**NOTE: The reference plane is the boundary, both physically and electrically, between the calibrated and uncalibrated portions of the circuit. Everything outside the reference plane is considered part of the DUT. Any instrument that does not use calibration or de-embedding of the test fixture defines the DUT as the total of externally connected components. If the de-embedding file is not used, all of the PCIeM2-TPA2 and associated coaxial cables, as well as cables connecting the TPA assembly to the test instrument, would be a part of the DUT.**

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Non-repeatable errors, such as drift or random errors, can be reduced but not corrected. Drift errors aggregate over time or with environmental changes such as temperature shift. To eliminate drift errors, perform an instrumentation-level calibration.

A random error cannot be corrected through calibration since the error occurred randomly. Random errors are typically associated with either test instrument noise or test repeatability problems. Reduce test instrument noise by increasing source power, lowering the IF bandwidth, or averaging results over multiple sweeps. Reduce test repeatability problems through the use of a torque wrench or, again, by averaging over multiple sweeps.

## Mechanical and Environmental Specifications

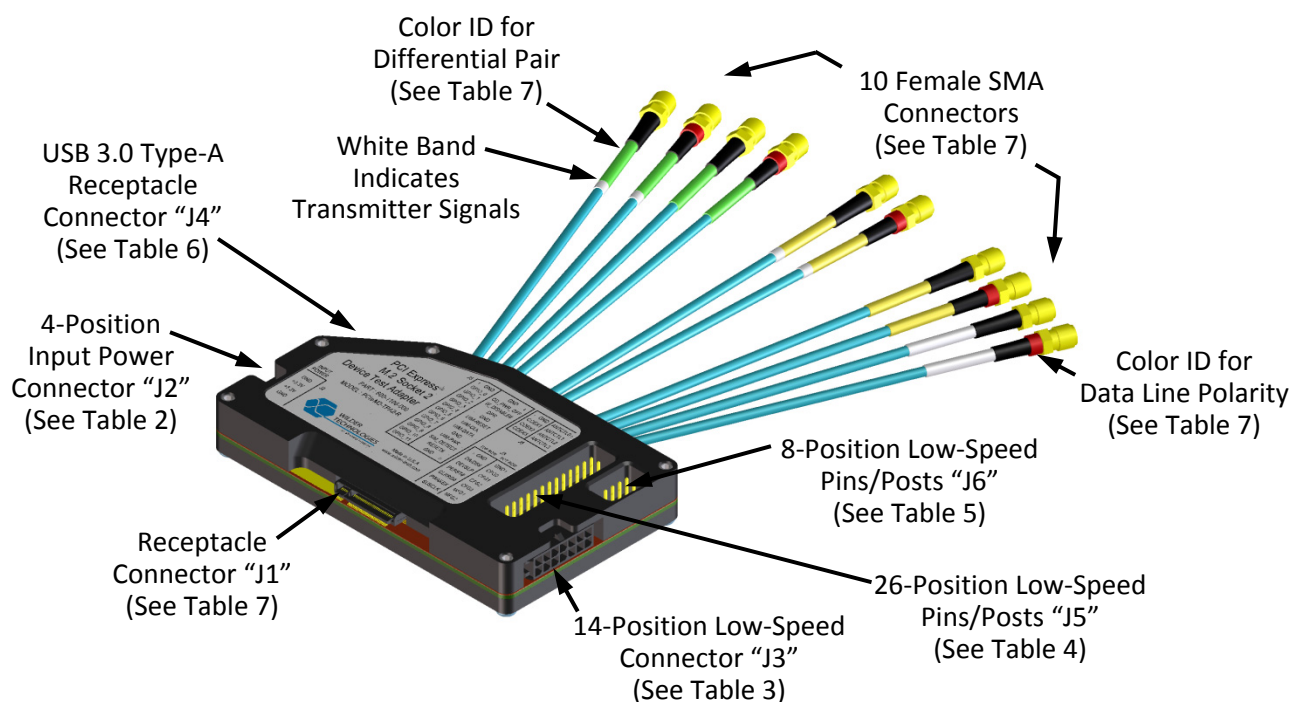
**NOTE: All specifications in this manual are subject to change.**

**Table 1. General Specifications**

| ITEM                                       | DESCRIPTION                                                 |
|--------------------------------------------|-------------------------------------------------------------|
| Usage Environment                          | Controlled indoor environment                               |
| Host Test Adapter Length (w/std. cables)   | 187mm +/- 2mm (7.36 inches +/- .08 inches) (Characteristic) |
| Device Test Adapter Length (w/std. cables) | 199mm +/- 2mm (7.84 inches +/- .08 inches) (Characteristic) |
| Operating Temperature                      | 0°C to +55°C (32°F to +131°F) (Characteristic)              |
| Storage Temperature                        | -40°C to +70°C (-40°F to +158°F) (Characteristic)           |

### PCIe M.2 Socket 2 Device TPA (PCIeM2-TPA2-R) Cable Pinout

The PCIeM2-TPA2-R cables provide 10 SMA connectors (two lanes of primary differential receive and transmit, and reference clock), one 4-position input power connector, three connectors containing the low-speed signals, and one USB 3.0 Type-A receptacle connector with SuperSpeed disabled. Labels clearly mark each cable or connector. The following figure refers to pin-description tables for each of the connector types. Note: The input power supply (3.3V) has a 22µF in parallel with two-each 0.01µF capacitors.



**Figure 3. Cable Connectors (PCIeM2-TPA2-R shown)**

**Table 2. PCIe M.2 Socket 2 Device TPA 4-Position Input Power Connector “J2”**

| LABEL | PIN NO. | DESCRIPTION |
|-------|---------|-------------|
| GND   | Pin 1   | Ground      |
| +3.3V | Pin 2   | +3.3 Volts  |
| +3.3V | Pin 3   | +3.3 Volts  |
| GND   | Pin 4   | Ground      |

**Table 3. PCIe M.2 Socket 2 Device TPA 14-Position Low-Speed Connector “J3”**

| LABEL  | PIN NO. | DESCRIPTION                                                                      |
|--------|---------|----------------------------------------------------------------------------------|
| GND    | Pin 1   | Ground                                                                           |
| CFG0   | Pin 2   | Configuration 0                                                                  |
| CFG1   | Pin 3   | Configuration 1                                                                  |
| CFG2   | Pin 4   | Configuration 2                                                                  |
| CFG3   | Pin 5   | Configuration 3                                                                  |
| MFG1   | Pin 6   | Vendor Specific / Manufacturing Pin                                              |
| MFG2   | Pin 7   | Vendor Specific / Manufacturing Pin                                              |
| GND    | Pin 8   | Ground                                                                           |
| DA/DS# | Pin 9   | Drive Activity Signal (active-high), Disable Staggered Spin-Up (active-low)      |
| DEVSLP | Pin 10  | Device Sleep                                                                     |
| PERST# | Pin 11  | PE-Reset (Functional Reset) (active-low)                                         |
| CLKRQ# | Pin 12  | Clock Request (active-low)                                                       |
| PWAKE# | Pin 13  | PCIe PME Wake (active-low)                                                       |
| SUSCLK | Pin 14  | Suspend Clock is a 32.768 kHz clock input that is provided by the user as needed |

**Table 4. PCIe M.2 Socket 2 Device TPA 26-Position Low-Speed Pins/Posts “J5”**

| <b>LABEL</b> | <b>PIN NO.</b> | <b>DESCRIPTION</b>                                        |
|--------------|----------------|-----------------------------------------------------------|
| GND          | Pin 1          | Ground                                                    |
| GND          | Pin 2          | Ground                                                    |
| GPIO_0       | Pin 3          | General Purpose Input/Output 0 (Configuration Dependent)  |
| CD_PW_OFF#   | Pin 4          | Full Card Power Off#                                      |
| GPIO_1       | Pin 5          | General Purpose Input/Output 1 (Configuration Dependent)  |
| W_DISABLE#   | Pin 6          | Wireless Disable Signal 1#                                |
| GPIO_2       | Pin 7          | General Purpose Input/Output 2 (Configuration Dependent)  |
| DPR          | Pin 8          | Dynamic Power Reduction                                   |
| GPIO_3       | Pin 9          | General Purpose Input/Output 3 (Configuration Dependent)  |
| GND          | Pin 10         | Ground                                                    |
| GPIO_4       | Pin 11         | General Purpose Input/Output 4 (Configuration Dependent)  |
| UIM-RESET    | Pin 12         | UIM Reset Signal                                          |
| GPIO_5       | Pin 13         | General Purpose Input/Output 5 (Configuration Dependent)  |
| UIM-CLK      | Pin 14         | UIM Clock Signal                                          |
| GPIO_6       | Pin 15         | General Purpose Input/Output 6 (Configuration Dependent)  |
| UIM-DATA     | Pin 16         | UIM Data Signal                                           |
| GPIO_7       | Pin 17         | General Purpose Input/Output 7 (Configuration Dependent)  |
| GND          | Pin 18         | Ground                                                    |
| GPIO_8       | Pin 19         | General Purpose Input/Output 8 (Configuration Dependent)  |
| UIM-PWR      | Pin 20         | UIM Power Source                                          |
| GPIO_9       | Pin 21         | General Purpose Input/Output 9 (Configuration Dependent)  |
| SIM_DETECT   | Pin 22         | Detects SIM Insertion/Removal                             |
| GPIO_10      | Pin 23         | General Purpose Input/Output 10 (Configuration Dependent) |
| RESET#       | Pin 24         | A single control to Reset the WWAN solution               |
| GPIO_11      | Pin 25         | General Purpose Input/Output 11 (Configuration Dependent) |
| GND          | Pin 26         | Ground                                                    |

**Table 5. PCIe M.2 Socket 2 Device TPA 8-Position Low-Speed Pins/Posts “J6”**

| <b>LABEL</b> | <b>PIN NO.</b> | <b>DESCRIPTION</b>       |
|--------------|----------------|--------------------------|
| GND          | Pin 1          | Ground                   |
| ANTCTL0      | Pin 2          | Antenna Control Signal 0 |
| COEX1        | Pin 3          | Coexistence Signal 1     |
| ANTCTL1      | Pin 4          | Antenna Control Signal 1 |
| COEX2        | Pin 5          | Coexistence Signal 2     |
| ANTCTL2      | Pin 6          | Antenna Control Signal 2 |
| COEX3        | Pin 7          | Coexistence Signal 3     |
| ANTCTL3      | Pin 8          | Antenna Control Signal 3 |

**Table 6. PCIe M.2 Socket 2 Device USB 3.0 Type-A Receptacle Connector “J4”  
(SuperSpeed Disabled)**

| <b>PIN NO.</b> | <b>DESCRIPTION</b>                                                      |
|----------------|-------------------------------------------------------------------------|
| Pin 1          | VBUS (Bypassed with 2200pF Capacitor to Ground)                         |
| Pin 2          | D-                                                                      |
| Pin 3          | D+                                                                      |
| Pin 4          | Ground                                                                  |
| Pin 5          | StdA_SSRX- (Disabled. Terminated to Ground through a 45.3 Ohm Resistor) |
| Pin 6          | StdA_SSRX+ (Disabled. Terminated to Ground through a 45.3 Ohm Resistor) |
| Pin 7          | GND_DRAIN (Ground)                                                      |
| Pin 8          | StdA_SSTX- (Disabled. Terminated to Ground through a 45.3 Ohm Resistor) |
| Pin 9          | StdA_SSTX+ (Disabled. Terminated to Ground through a 45.3 Ohm Resistor) |
| Shell          | Shield (Connector Shell)                                                |



**Table 7. PCIe M.2 Socket 2 Device TPA (Receptacle) Pin Assignments**

| Pin Description                            | Connector Pin Number                     | Destination Number         | Color ID for Data Line Polarity | Color ID for Differential Pair (Receptacle) |
|--------------------------------------------|------------------------------------------|----------------------------|---------------------------------|---------------------------------------------|
| Configuration 3                            | 1                                        | CFG3                       | N/A                             | N/A                                         |
| +3.3 Volts                                 | 2, 4, 70, 72, 74                         | +3.3V                      | N/A                             | N/A                                         |
| Ground                                     | 3, 5, 11, 27, 33, 39, 45, 51, 57, 71, 73 | GND                        | N/A                             | N/A                                         |
| FULL_CARD_POWER_OFF#                       | 6                                        | CD_PWR_OFF                 | N/A                             | N/A                                         |
| USB_D+                                     | 7                                        | USB_D+ (No Marking)        | N/A                             | N/A                                         |
| W_DISABLE1#                                | 8                                        | W_DISABLE#                 | N/A                             | N/A                                         |
| USB_D-                                     | 9                                        | USB_D- (No Marking)        | N/A                             | N/A                                         |
| GPIO_9-LED_1#/DAS/DSS#                     | 10                                       | DA/DS# (J3)<br>GPIO_9 (J5) | N/A                             | N/A                                         |
| Key-B                                      | 12, 13, 14, 15, 16, 17, 18, 19           | N/A                        | N/A                             | N/A                                         |
| General Purpose I/O_5                      | 20                                       | GPIO_5                     | N/A                             | N/A                                         |
| Configuration 0                            | 21                                       | CFG0                       | N/A                             | N/A                                         |
| General Purpose I/O_6                      | 22                                       | GPIO_6                     | N/A                             | N/A                                         |
| General Purpose I/O_11                     | 23                                       | GPIO_11                    | N/A                             | N/A                                         |
| General Purpose I/O_7                      | 24                                       | GPIO_7                     | N/A                             | N/A                                         |
| Dynamic Power Reduction                    | 25                                       | DPR                        | N/A                             | N/A                                         |
| General Purpose I/O_10                     | 26                                       | GPIO_10                    | N/A                             | N/A                                         |
| General Purpose I/O_8                      | 28                                       | GPIO_8                     | N/A                             | N/A                                         |
| PETn1 (Device Test Transmitter 1 Negative) | 29                                       | DEV PET1-                  | Black                           | Green/Wht Band                              |
| UIM_RESET                                  | 30                                       | UIM-RESET                  | N/A                             | N/A                                         |
| PETp1 (Device Test Transmitter 1 Positive) | 31                                       | DEV PET1+                  | Red                             | Green/Wht Band                              |
| UIM_CLK                                    | 32                                       | UIM-CLK                    | N/A                             | N/A                                         |
| UIM_DATA                                   | 34                                       | UIM-DATA                   | N/A                             | N/A                                         |
| PERn1 (Device Test Receiver 1 Negative)    | 35                                       | DEV PER1-                  | Black                           | Green                                       |
| UIM_PWR                                    | 36                                       | UIM-PWR                    | N/A                             | N/A                                         |
| PERp1 (Device Test Receiver 1 Positive)    | 37                                       | DEV PER1+                  | Red                             | Green                                       |
| DEVSLP (Device Sleep)                      | 38                                       | DEVSLP                     | N/A                             | N/A                                         |
| General Purpose I/O_0                      | 40                                       | GPIO_0                     | N/A                             | N/A                                         |



| Pin Description                             | Connector Pin Number | Destination Number | Color ID for Data Line Polarity | Color ID for Differential Pair (Receptacle) |
|---------------------------------------------|----------------------|--------------------|---------------------------------|---------------------------------------------|
| PETn0 (Device Test Transmitter 0 Negative)  | 41                   | DEV PET0-          | Black                           | Yellow/Wht Band                             |
| General Purpose I/O _1                      | 42                   | GPIO_1             | N/A                             | N/A                                         |
| PETp0 (Device Test Transmitter 0 Positive)  | 43                   | DEV PET0+          | Red                             | Yellow/Wht Band                             |
| General Purpose I/O _2                      | 44                   | GPIO_2             | N/A                             | N/A                                         |
| General Purpose I/O _3                      | 46                   | GPIO_3             | N/A                             | N/A                                         |
| PERn0 (Device Test Receiver 0 Negative)     | 47                   | DEV PER0-          | Black                           | Yellow                                      |
| General Purpose I/O _4                      | 48                   | GPIO_4             | N/A                             | N/A                                         |
| PERp0 (Device Test Receiver 0 Positive)     | 49                   | DEV PER0+          | Red                             | Yellow                                      |
| PERST# (PE-Reset)                           | 50                   | PERST#             | N/A                             | N/A                                         |
| CLKREQ# (Clock Request)                     | 52                   | CLKRQ#             | N/A                             | N/A                                         |
| REFCLKN                                     | 53                   | DEV RCLK-          | Black                           | White                                       |
| PEWAKE# (PCIe PME Wake)                     | 54                   | PWAKE#             | N/A                             | N/A                                         |
| REFCLKP                                     | 55                   | DEV RCLK+          | Red                             | White                                       |
| MFG-1 (Vendor Specific / Manufacturing Pin) | 56                   | MFG1               | N/A                             | N/A                                         |
| MFG-2 (Vendor Specific / Manufacturing Pin) | 58                   | MFG2               | N/A                             | N/A                                         |
| ANTCTL0 (Antenna Control 0)                 | 59                   | ANTCTL0            | N/A                             | N/A                                         |
| COEX3 (Coexistence 3)                       | 60                   | COEX3              | N/A                             | N/A                                         |
| ANTCTL1 (Antenna Control 1)                 | 61                   | ANTCTL1            | N/A                             | N/A                                         |
| COEX2 (Coexistence 2)                       | 62                   | COEX2              | N/A                             | N/A                                         |
| ANTCTL2 (Antenna Control 2)                 | 63                   | ANTCTL2            | N/A                             | N/A                                         |
| COEX1 (Coexistence 1)                       | 64                   | COEX1              | N/A                             | N/A                                         |
| ANTCTL3 (Antenna Control 3)                 | 65                   | ANTCTL3            | N/A                             | N/A                                         |
| SIM_DETECT (SIM Card Detect)                | 66                   | SIM_DETECT         | N/A                             | N/A                                         |
| RESET# (Resets WWAN)                        | 67                   | RESET#             | N/A                             | N/A                                         |
| SUSCLK (Suspend Clock)                      | 68                   | SUSCLK             | N/A                             | N/A                                         |
| Configuration 1                             | 69                   | CFG1               | N/A                             | N/A                                         |
| Configuration 2                             | 75                   | CFG2               | N/A                             | N/A                                         |

### PCIeM2-TPA2-P Cable Pinout

The PCIeM2-TPA2-P cables provide 10 SMA connectors (two lanes of primary differential receive and transmit, and reference clock), one USB 3.0 Type-A receptacle connector with SuperSpeed disabled. Labels clearly mark each SMA cable. The following figure refers to the pin-description tables for the USB type-A connector and the M.2 primary connector.

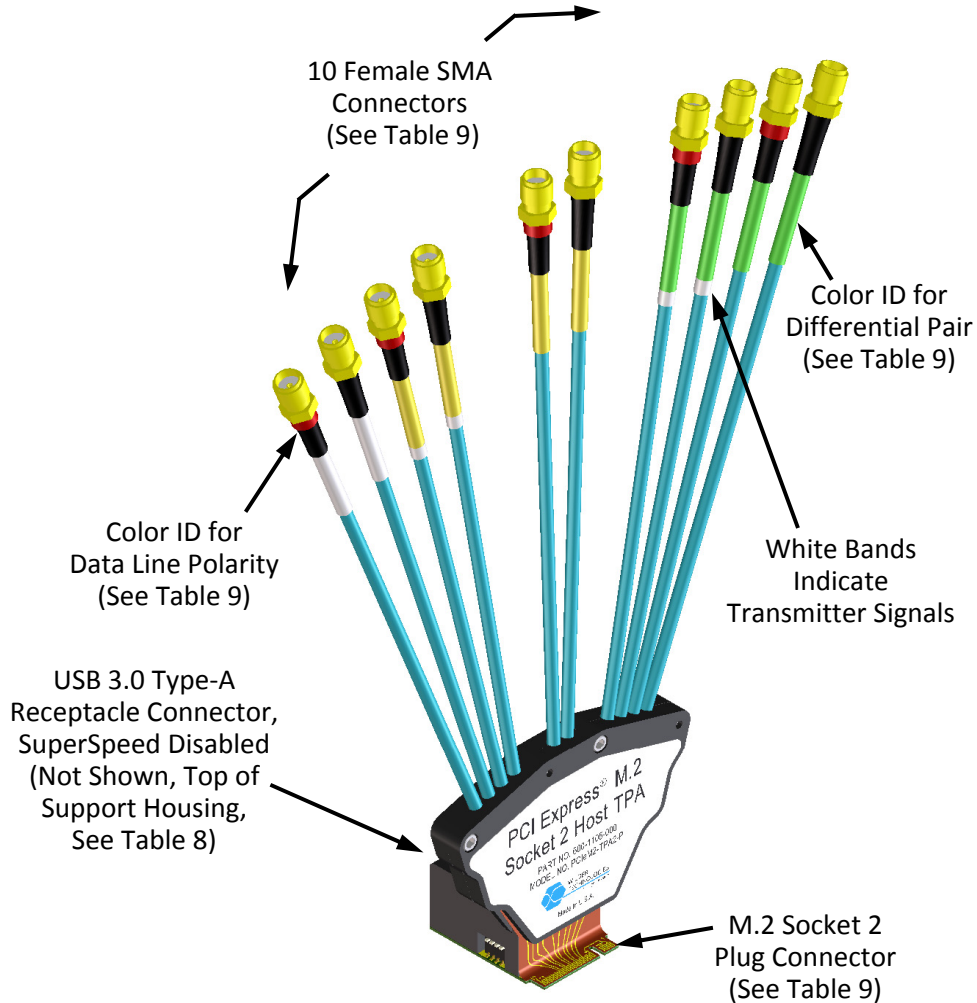


Figure 4. Cable Connectors (PCIeM2-TPA2-P shown)

Table 8. PCIe M.2 Socket 2 Host USB 3.0 Type-A Receptacle Connector (SuperSpeed Disabled)

| PIN NO. | DESCRIPTION                                                             |
|---------|-------------------------------------------------------------------------|
| Pin 1   | VBUS (Bypassed with 2200pF Capacitor to Ground)                         |
| Pin 2   | D-                                                                      |
| Pin 3   | D+                                                                      |
| Pin 4   | Ground                                                                  |
| Pin 5   | StdA_SSRX- (Disabled. Terminated to Ground through a 45.3 Ohm Resistor) |
| Pin 6   | StdA_SSRX+ (Disabled. Terminated to Ground through a 45.3 Ohm Resistor) |
| Pin 7   | GND_DRAIN (Ground)                                                      |
| Pin 8   | StdA_SSTX- (Disabled. Terminated to Ground through a 45.3 Ohm Resistor) |
| Pin 9   | StdA_SSTX+ (Disabled. Terminated to Ground through a 45.3 Ohm Resistor) |
| Shell   | Shield (Connector Shell)                                                |

**Table 9. PCIe M.2 Socket 2 Host TPA (Plug) Pin Assignments**

| Pin Description                          | Connector Pin Number                     | Destination Number  | Color ID for Data Line Polarity | Color ID for Differential Pair (Plug) |
|------------------------------------------|------------------------------------------|---------------------|---------------------------------|---------------------------------------|
| Configuration 3                          | 1                                        | Switch 1, Pos. 4    | N/A                             | N/A                                   |
| +3.3 Volts                               | 2, 4, 70, 72, 74                         | No Connect          | N/A                             | N/A                                   |
| Ground                                   | 3, 5, 11, 27, 33, 39, 45, 51, 57, 71, 73 | GND                 | N/A                             | N/A                                   |
| FULL_CARD_POWER_OFF#                     | 6                                        | No Connect          | N/A                             | N/A                                   |
| USB_D+                                   | 7                                        | USB_D+ (No Marking) | N/A                             | N/A                                   |
| W_DISABLE1#                              | 8                                        | No Connect          | N/A                             | N/A                                   |
| USB_D-                                   | 9                                        | USB_D- (No Marking) | N/A                             | N/A                                   |
| GPIO_9-LED_1#/DAS/DSS#                   | 10                                       | No Connect          | N/A                             | N/A                                   |
| Key-B                                    | 12, 13, 14, 15, 16, 17, 18, 19           | N/A                 | N/A                             | N/A                                   |
| General Purpose I/O_5                    | 20                                       | No Connect          | N/A                             | N/A                                   |
| Configuration 0                          | 21                                       | Switch 1, Pos. 1    | N/A                             | N/A                                   |
| General Purpose I/O_6                    | 22                                       | No Connect          | N/A                             | N/A                                   |
| General Purpose I/O_11                   | 23                                       | No Connect          | N/A                             | N/A                                   |
| General Purpose I/O_7                    | 24                                       | No Connect          | N/A                             | N/A                                   |
| Dynamic Power Reduction                  | 25                                       | No Connect          | N/A                             | N/A                                   |
| General Purpose I/O_10                   | 26                                       | No Connect          | N/A                             | N/A                                   |
| General Purpose I/O_8                    | 28                                       | No Connect          | N/A                             | N/A                                   |
| PERn1 (Host Test Receiver 1 Negative)    | 29                                       | HOST PER1-          | Black                           | Green                                 |
| UIM_RESET                                | 30                                       | No Connect          | N/A                             | N/A                                   |
| PERp1 (Host Test Receiver 1 Positive)    | 31                                       | HOST PER1+          | Red                             | Green                                 |
| UIM_CLK                                  | 32                                       | No Connect          | N/A                             | N/A                                   |
| UIM_DATA                                 | 34                                       | No Connect          | N/A                             | N/A                                   |
| PETn1 (Host Test Transmitter 1 Negative) | 35                                       | HOST PET1-          | Black                           | Green/Wht Band                        |
| UIM_PWR                                  | 36                                       | No Connect          | N/A                             | N/A                                   |
| PETp1 (Host Test Transmitter 1 Positive) | 37                                       | HOST PET1+          | Red                             | Green/Wht Band                        |
| DEVSLP (Device Sleep)                    | 38                                       | No Connect          | N/A                             | N/A                                   |
| General Purpose I/O_0                    | 40                                       | No Connect          | N/A                             | N/A                                   |



**Table 9. PCIe M.2 Socket 2 Host TPA (Plug) Pin Assignments (Continued)**

| Pin Description                             | Connector Pin Number | Destination Number | Color ID for Data Line Polarity | Color ID for Differential Pair (Plug) |
|---------------------------------------------|----------------------|--------------------|---------------------------------|---------------------------------------|
| PERn0 (Host Test Receiver 0 Negative)       | 41                   | HOST PER0-         | Black                           | Yellow                                |
| General Purpose I/O _1                      | 42                   | No Connect         | N/A                             | N/A                                   |
| PERp0 (Host Test Receiver 0 Positive)       | 43                   | HOST PER0+         | Red                             | Yellow                                |
| General Purpose I/O _2                      | 44                   | No Connect         | N/A                             | N/A                                   |
| General Purpose I/O _3                      | 46                   | No Connect         | N/A                             | N/A                                   |
| PETn0 (Host Test Transmitter 0 Negative)    | 47                   | HOST PET0-         | Black                           | Yellow/Wht Band                       |
| General Purpose I/O _4                      | 48                   | No Connect         | N/A                             | N/A                                   |
| PETp0 (Host Test Transmitter 0 Positive)    | 49                   | HOST PET0+         | Red                             | Yellow/Wht Band                       |
| PERST# (PE-Reset)                           | 50                   | No Connect         | N/A                             | N/A                                   |
| CLKREQ# (Clock Request)                     | 52                   | No Connect         | N/A                             | N/A                                   |
| REFCLKN                                     | 53                   | HOST RCLK-         | Black                           | White                                 |
| PEWAKE# (PCIe PME Wake)                     | 54                   | No Connect         | N/A                             | N/A                                   |
| REFCLKP                                     | 55                   | HOST RCLK+         | Red                             | White                                 |
| MFG-1 (Vendor Specific / Manufacturing Pin) | 56                   | No Connect         | N/A                             | N/A                                   |
| MFG-2 (Vendor Specific / Manufacturing Pin) | 58                   | No Connect         | N/A                             | N/A                                   |
| ANTCTL0 (Antenna Control 0)                 | 59                   | No Connect         | N/A                             | N/A                                   |
| COEX3 (Coexistence 3)                       | 60                   | No Connect         | N/A                             | N/A                                   |
| ANTCTL1 (Antenna Control 1)                 | 61                   | No Connect         | N/A                             | N/A                                   |
| COEX2 (Coexistence 2)                       | 62                   | No Connect         | N/A                             | N/A                                   |
| ANTCTL2 (Antenna Control 2)                 | 63                   | No Connect         | N/A                             | N/A                                   |
| COEX1 (Coexistence 1)                       | 64                   | No Connect         | N/A                             | N/A                                   |
| ANTCTL3 (Antenna Control 3)                 | 65                   | No Connect         | N/A                             | N/A                                   |
| SIM_DETECT (SIM Card Detect)                | 66                   | No Connect         | N/A                             | N/A                                   |
| RESET# (Resets WWAN)                        | 67                   | No Connect         | N/A                             | N/A                                   |
| SUSCLK (Suspend Clock)                      | 68                   | No Connect         | N/A                             | N/A                                   |
| Configuration 1                             | 69                   | Switch 1, Pos. 2   | N/A                             | N/A                                   |
| Configuration 2                             | 75                   | Switch 1, Pos. 3   | N/A                             | N/A                                   |



### PCIeM2-TPA2-P Configuration Switch (Switch 1)

The PCIeM2-TPA2-P provides a 4-position switch to allow users to configure the test adapter and the configuration signals. This switch provides the means to indicate the specific configuration of the test adapter as well as indication of whether the test adapter is present or not. The meaning of each of the 16 possible decodes is shown in the PCIe M.2 specification

The switch allows the user to designate which signals should either be grounded or left “No Connect” to build the decode required for a given test adapter configuration. Per the PCIe M.2 specification, the host must provide a pull up resistor for each of these signals.

The following figure illustrates the switch location and circuit locations (toggles) to designate each of the configuration pins (CONFIG[0..3]). Refer to the PCIe M.2 Specification for detailed, application specific settings of the configuration signals.

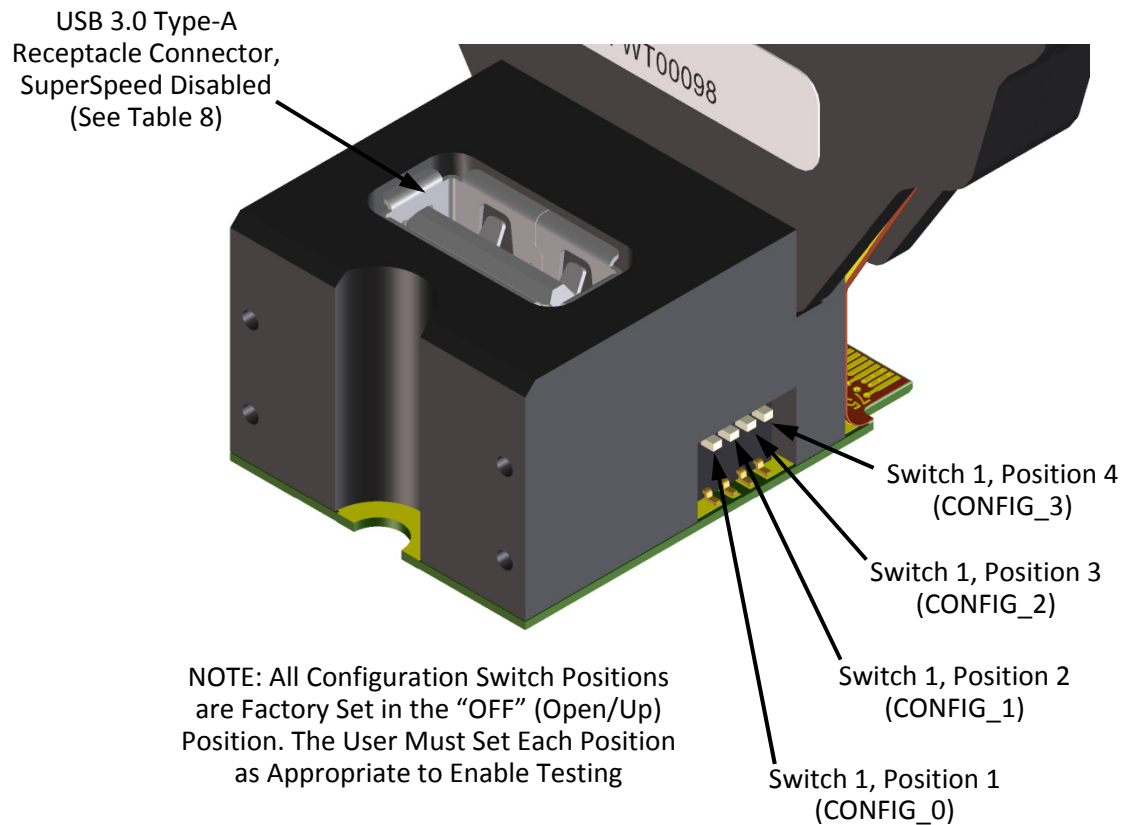


Figure 5. Configuration Switch (PCIeM2-TPA2-P shown)

## Electrical Specifications

**NOTE: All specifications in this manual are subject to change.**

**Table 10. Electrical Specifications**

| SPECIFICATION                                   | MINIMUM | TYPICAL | MAXIMUM | NOTES                                                                                                       |
|-------------------------------------------------|---------|---------|---------|-------------------------------------------------------------------------------------------------------------|
| Differential Impedance (ohms), 100 ps Rise Time | 94      |         | 106     | All Differential Pairs, Device TPA and Host TPA, excluding PCIe M.2 connector.                              |
| Differential Impedance (ohms), 100 ps Rise Time | 85      |         | 115     | All Differential Pairs, Device TPA and Host TPA, including PCIe M.2 connector.                              |
| Impedance (ohms), 100 ps Rise Time              | 47.5    |         | 52.5    | All Single-Ended High-Speed Signals, Device TPA and Host TPA, excluding PCIe M.2 connector.                 |
| Impedance (ohms), 30 ps Rise Time               | 46.5    |         | 53.5    | SMA Connectors                                                                                              |
| Intra-pair Skew (ps)                            | -6      |         | 6       | All Differential Pairs, Device TPA and Host TPA                                                             |
| Inter-pair Skew (ps)                            | -6      |         | 6       | All Differential Pairs, Device TPA and Host TPA                                                             |
| NEXT (db), at TBD GHz                           | -30     |         |         | All Differential Pairs, single aggressor, without PCIe M.2 connector, with six-inch cables and terminations |
| Current Carrying (A)                            | 2.5     |         |         | +3.3V Power                                                                                                 |



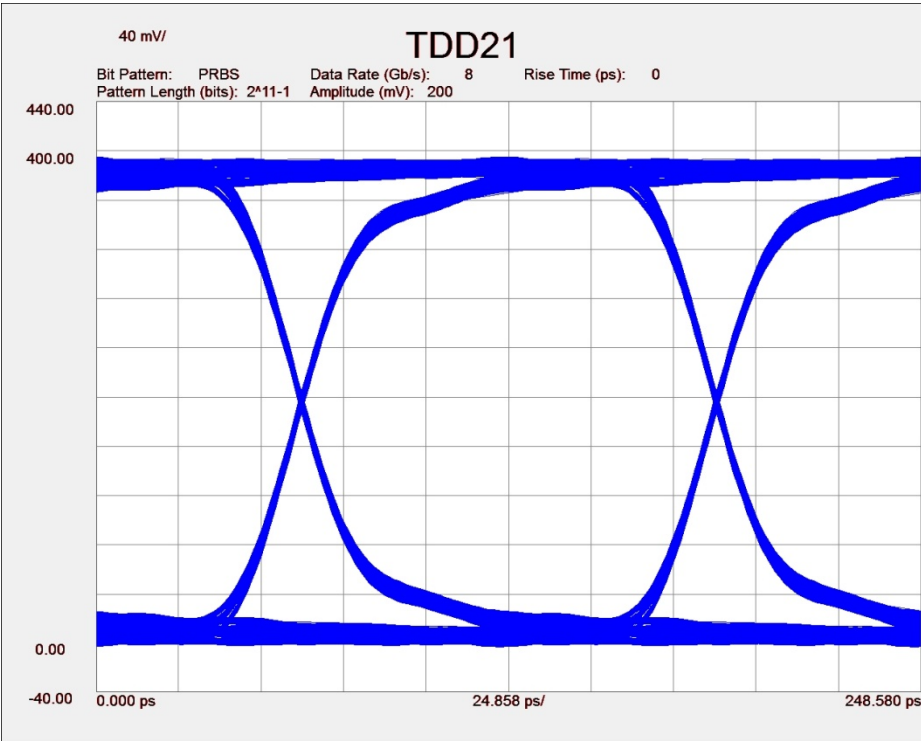
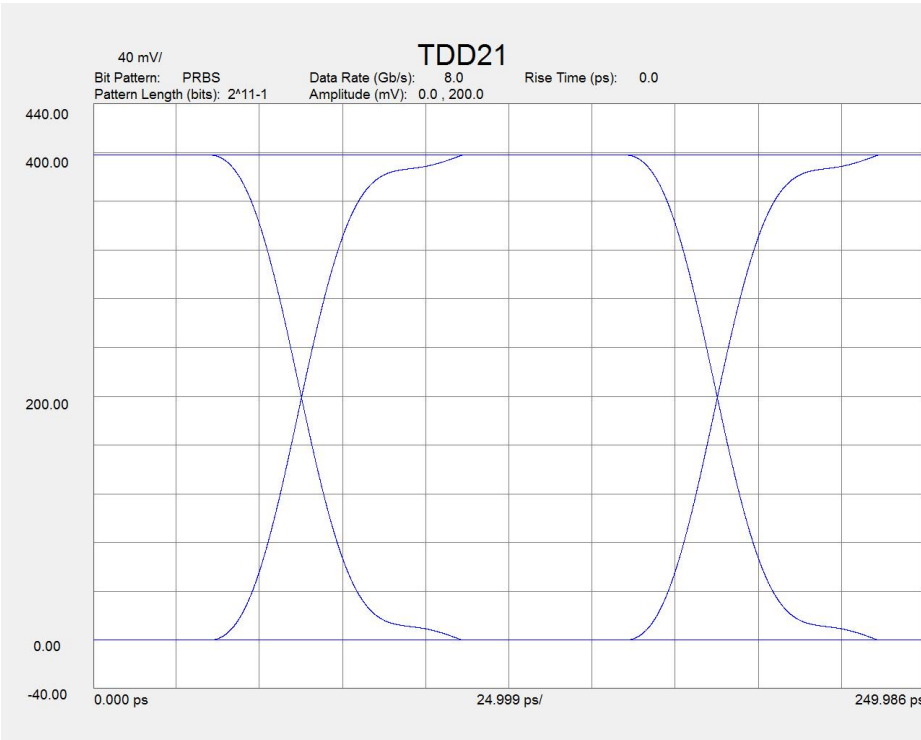


Figure 6. Typical mated pair 8 Gb/s eye diagram, with de-embedding (top) and without de-embedding (bottom)

| Parameter Measurement Result |          |
|------------------------------|----------|
| Name                         | Result   |
| Eye Level Zero (mV):         | 0.0000   |
| Eye Level One (mV):          | 397.8000 |
| Eye Level Mean (mV):         | 198.9000 |
| Eye Amplitude (mV):          | 397.8000 |
| Eye Height (mV):             | 397.8000 |
| Eye Height (dB):             | -0.0479  |
| Eye Width:                   | 125.0000 |
| Eye Opening Factor:          | 1.0000   |
| Eye Signal to Noise:         | 0.0000   |
| Eye Duty Cycle Dist:         | 0.0000   |
| Eye Duty Cycle Dist (%):     | 0.0000   |
| Eye Rise Time (10-90):       | 31.9307  |
| Eye Fall Time (10-90):       | 31.9429  |
| Eye Jitter (PP):             | 0.0000   |
| Eye Jitter (RMS):            | 0.0000   |

| Parameter Measurement Result |                    |
|------------------------------|--------------------|
| Name                         | Measurement Result |
| Eye Level Zero(mV)           | 13.27              |
| Eye Level One(mV)            | 379.27             |
| Eye Level Mean(mV)           | 196.27             |
| Eye Amplitude(mV)            | 366.00             |
| Eye Height(mV)               | 320.00             |
| Eye Height(db)               | -4.95              |
| Eye Width                    | 1.22e-010          |
| Eye Opening Factor           | 0.87               |
| Eye Signal_to_Noise          | 20.13              |
| Eye Duty Cycle Dist          | -5.55e-014         |
| Eye Duty Cycle Dist(%)       | -0.04              |
| Eye Rise Time (20-80)        | 2.53e-011          |
| Eye Fall Time (80-20)        | 2.53e-011          |
| Eye Jitter(PP)               | 3.05e-012          |
| Eye Jitter(RMS)              | 6.09e-013          |

Figure 7. Typical mated pair 8 Gb/s eye data, with de-embedding (top) and without de-embedding (bottom)

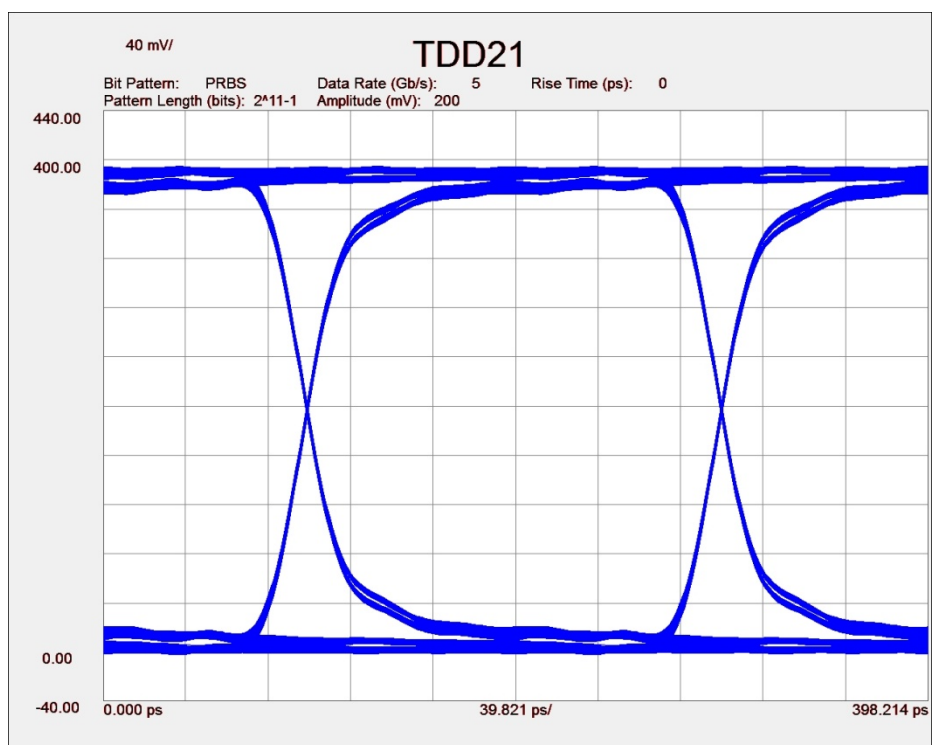
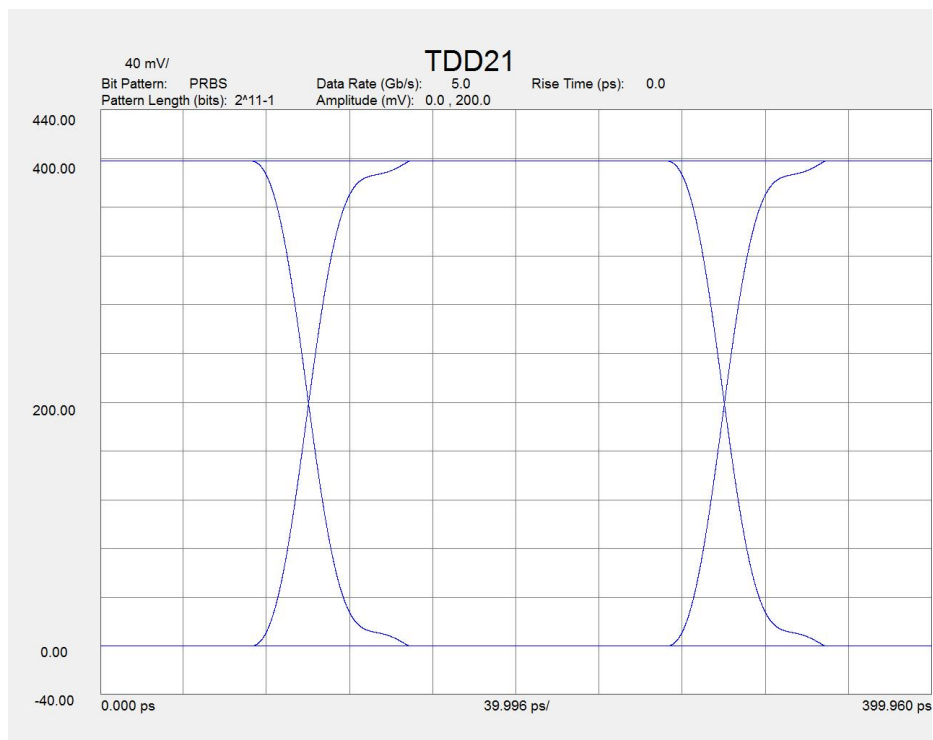


Figure 8. Typical mated pair 5 Gb/s eye diagram, with de-embedding (top) and without de-embedding (bottom)

| Parameter Measurement Result |          |
|------------------------------|----------|
| Name                         | Result   |
| Eye Level Zero (mV):         | 0.0000   |
| Eye Level One (mV):          | 397.8000 |
| Eye Level Mean (mV):         | 198.9000 |
| Eye Amplitude (mV):          | 397.8000 |
| Eye Height (mV):             | 397.8000 |
| Eye Height (dB):             | -0.0479  |
| Eye Width:                   | 197.1040 |
| Eye Opening Factor:          | 1.0000   |
| Eye Signal to Noise:         | 0.0000   |
| Eye Duty Cycle Dist:         | 0.0000   |
| Eye Duty Cycle Dist (%):     | 0.0000   |
| Eye Rise Time (10-90):       | 31.9106  |
| Eye Fall Time (10-90):       | 31.9233  |
| Eye Jitter (PP):             | 0.3225   |
| Eye Jitter (RMS):            | 0.4823   |

| Parameter Measurement Result |                    |
|------------------------------|--------------------|
| Name                         | Measurement Result |
| Eye Level Zero(mV)           | 10.12              |
| Eye Level One(mV)            | 383.27             |
| Eye Level Mean(mV)           | 196.69             |
| Eye Amplitude(mV)            | 373.15             |
| Eye Height(mV)               | 345.42             |
| Eye Height(db)               | -4.62              |
| Eye Width                    | 1.97e-010          |
| Eye Opening Factor           | 0.93               |
| Eye Signal_to_Noise          | 27.68              |
| Eye Duty Cycle Dist          | -1.93e-014         |
| Eye Duty Cycle Dist(%)       | -0.01              |
| Eye Rise Time (20-80)        | 2.60e-011          |
| Eye Fall Time (80-20)        | 2.60e-011          |
| Eye Jitter(PP)               | 3.10e-012          |
| Eye Jitter(RMS)              | 4.41e-013          |

Figure 9. Typical mated pair 12 Gb/s eye data, with de-embedding (top) and without de-embedding (bottom)

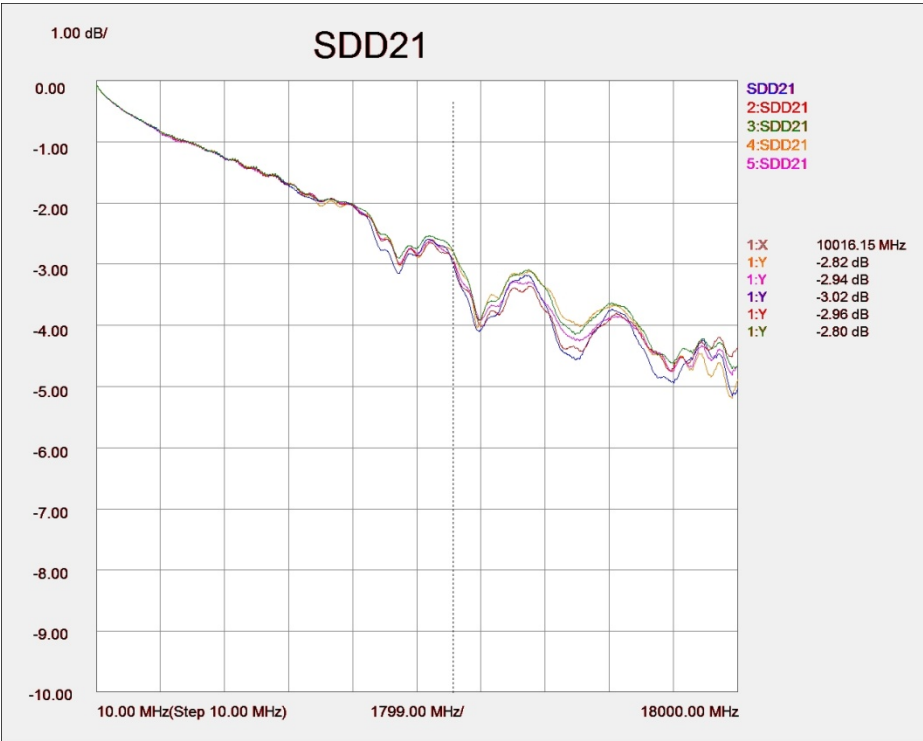
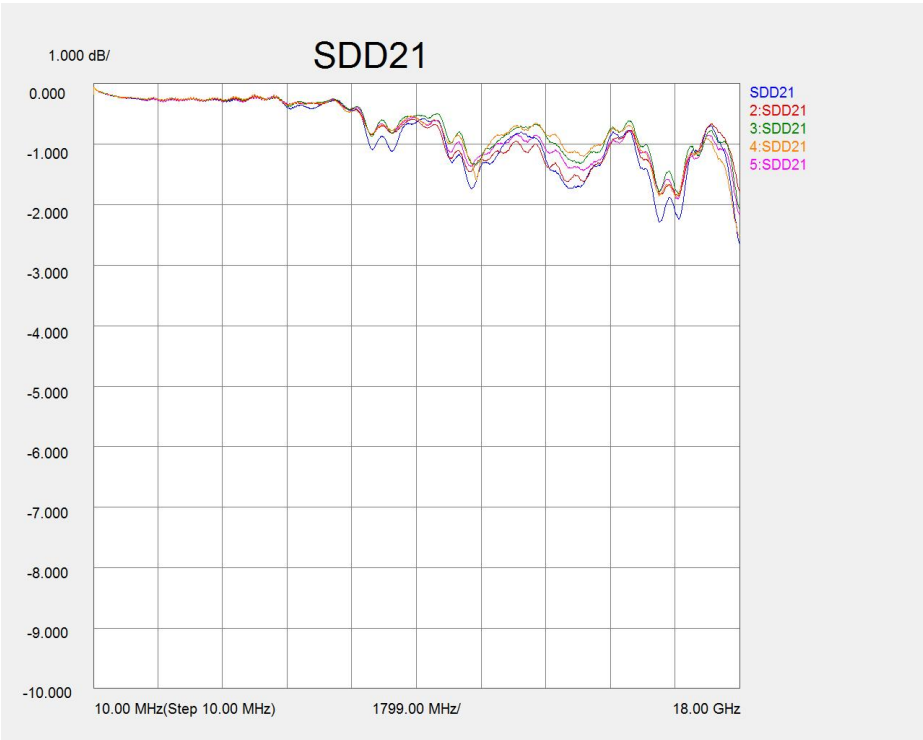


Figure 10. Typical mated pair balanced insertion loss, with de-embedding (top) and without de-embedding (bottom)

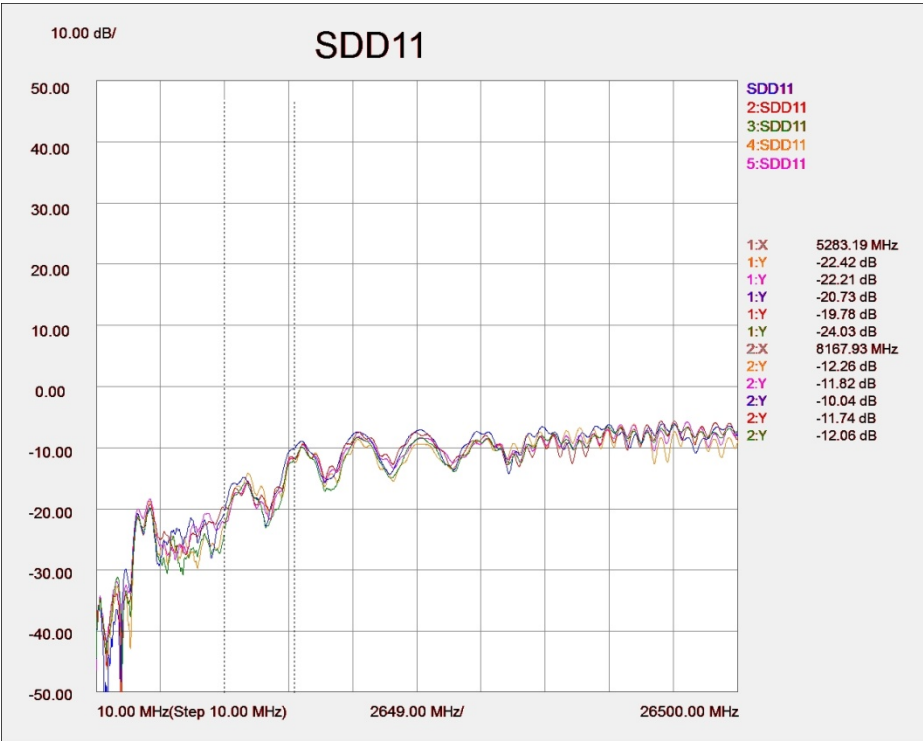
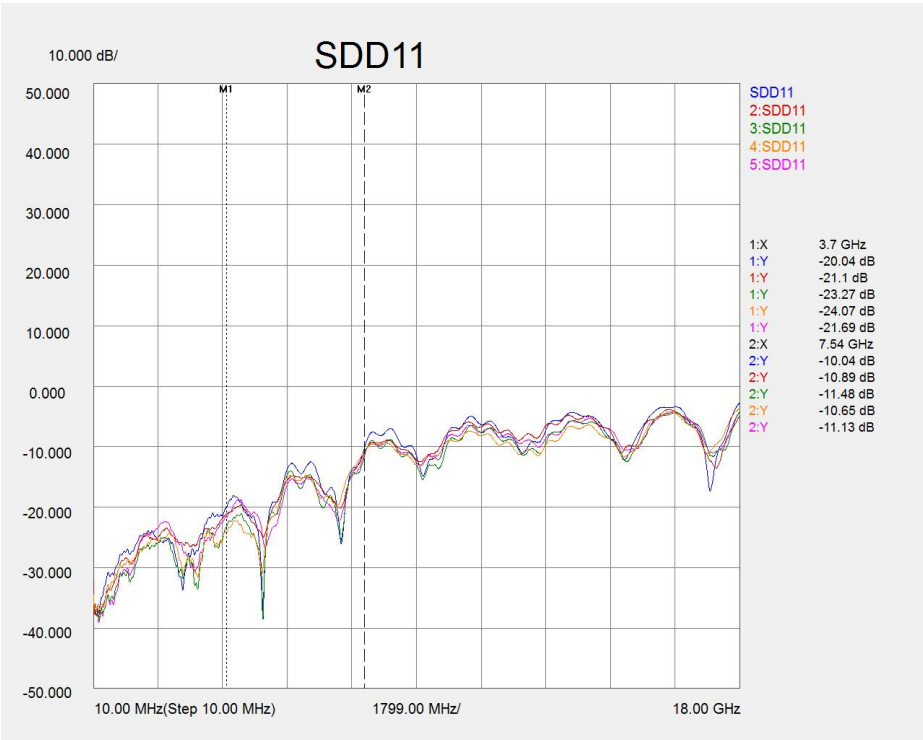


Figure 11. Typical mated pair balanced return loss, with de-embedding (top) and without de-embedding (bottom)

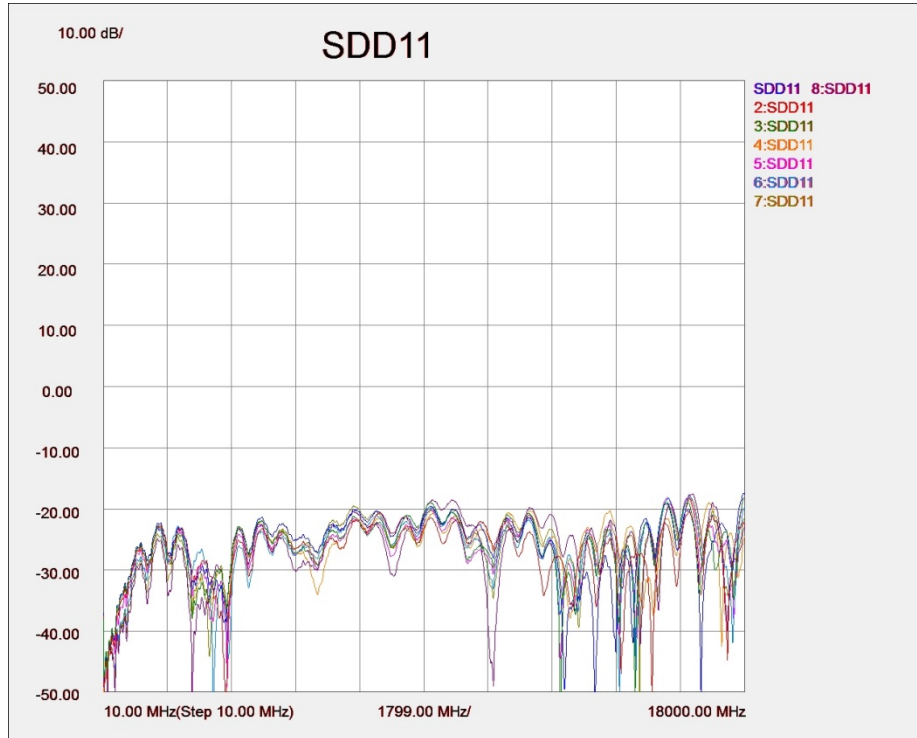


Figure 12. Typical TPA balanced return loss, differential termination replacing connector, M.2 socket 3 shown.

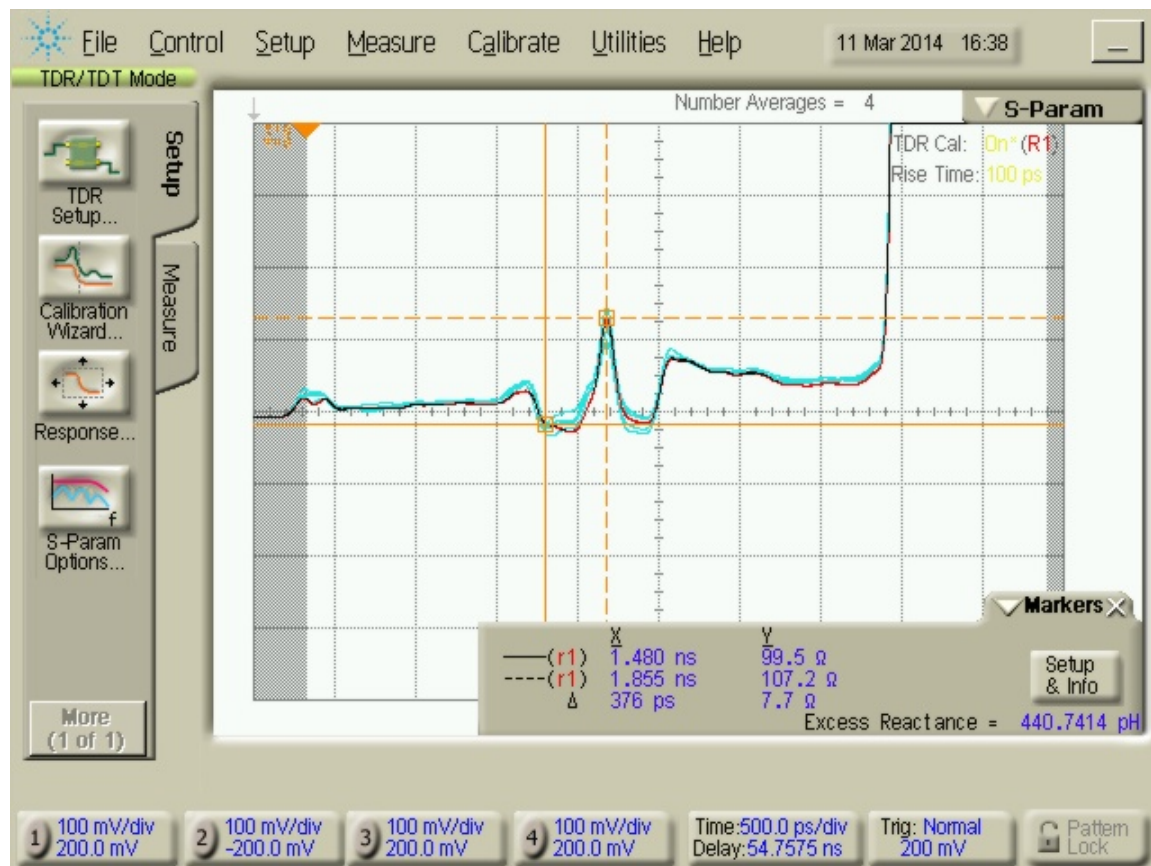


Figure 13. Typical differential TDR of TPA-P connected to TPA-R at 100 ps Rise Time, example differential pairs. (Equivalent to 70ps, 20% to 80%.)



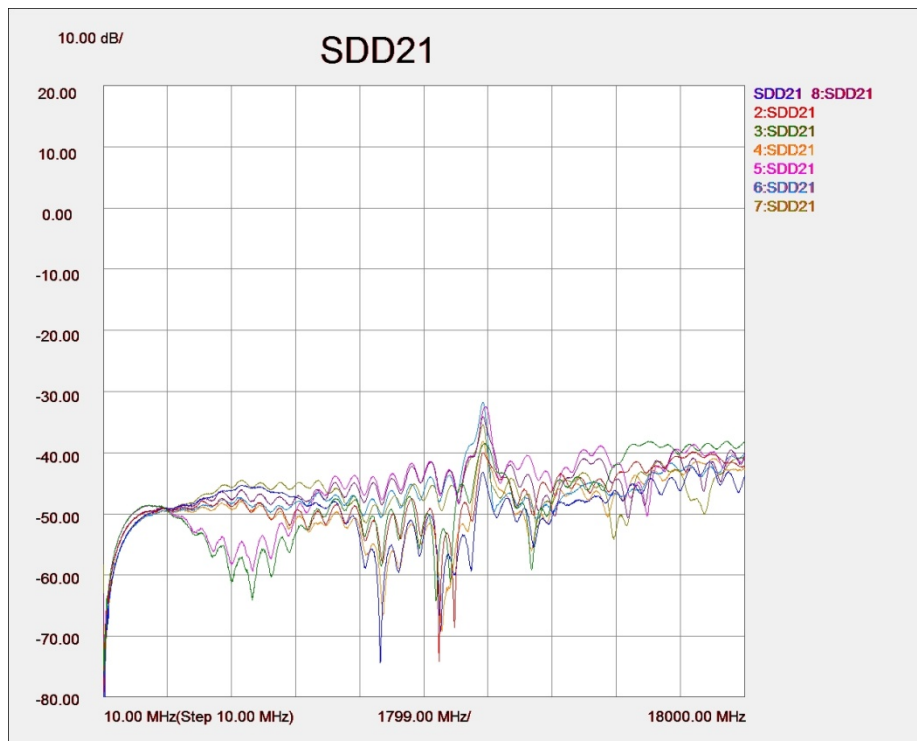
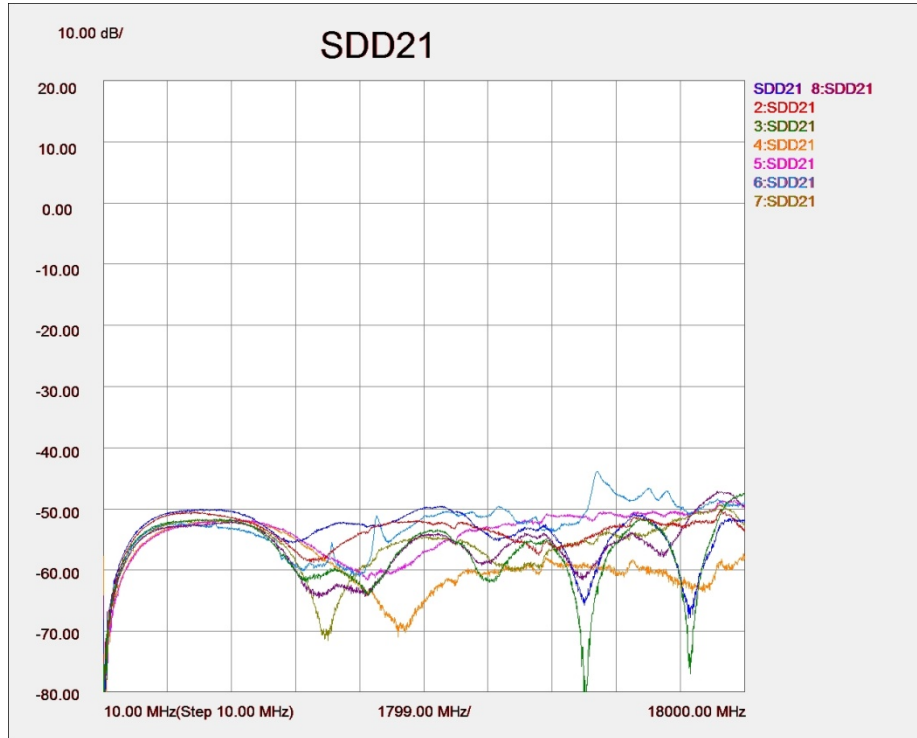


Figure 14. Typical Differential NEXT, without connector (top, socket 3 shown) and with mated connectors (bottom), adjacent differential pairs, all differential pairs terminated at both ends

## PCIe M.2 TPA Socket 2 Accessories and Optional Accessories

### PCIeM2-TPA2-R Accessories

The PCIeM2-TPA2-R (Device TPA) is supplied with Device Support Adapter materials that allow the user to properly retain and stabilize a device under test. (Ref. Wilder Technologies kit part number 600-1097-000.)

The figure, below, illustrates the installation and a typical application of the Device Support Adapter materials.

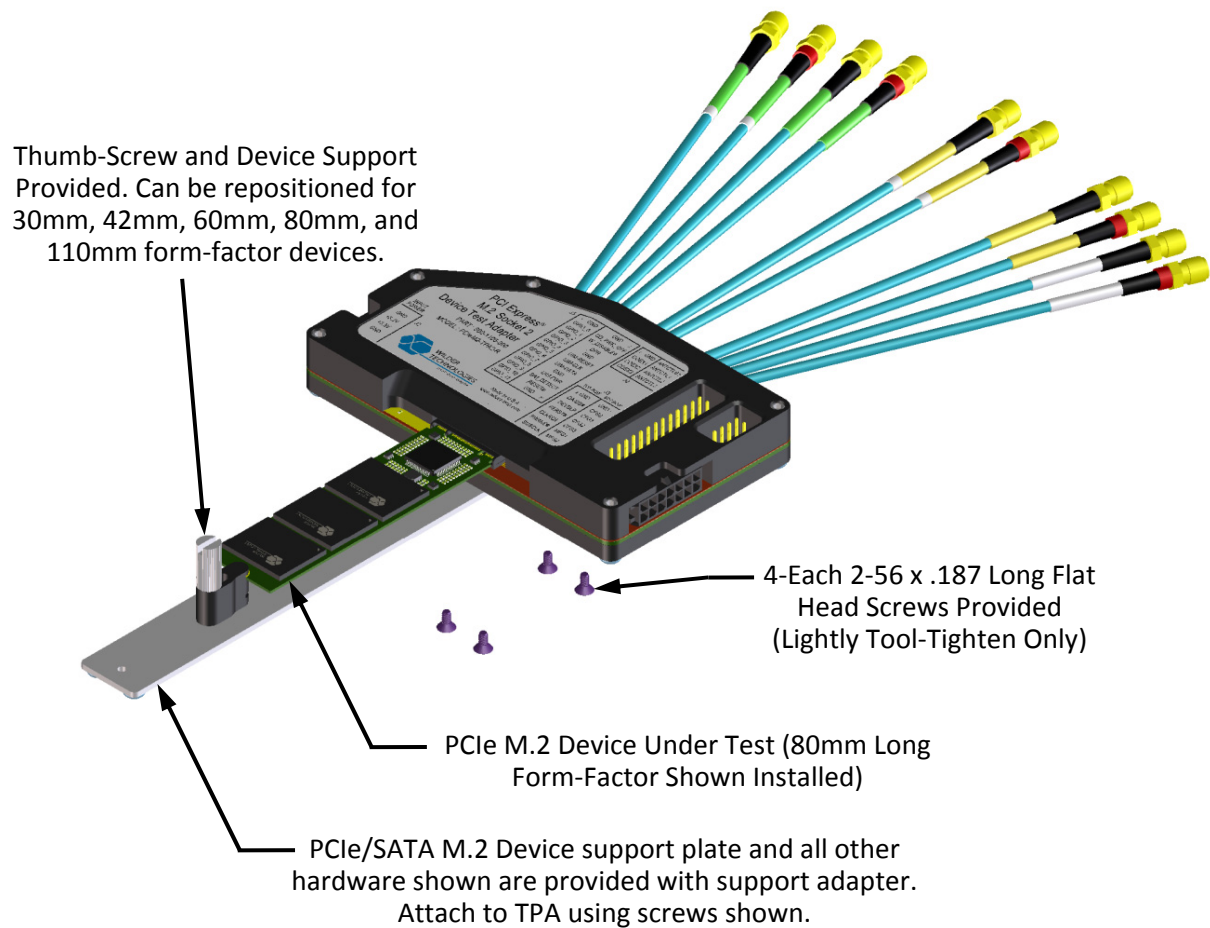


Figure 15. PCIeM2-TPA2-R Device Support Adapter

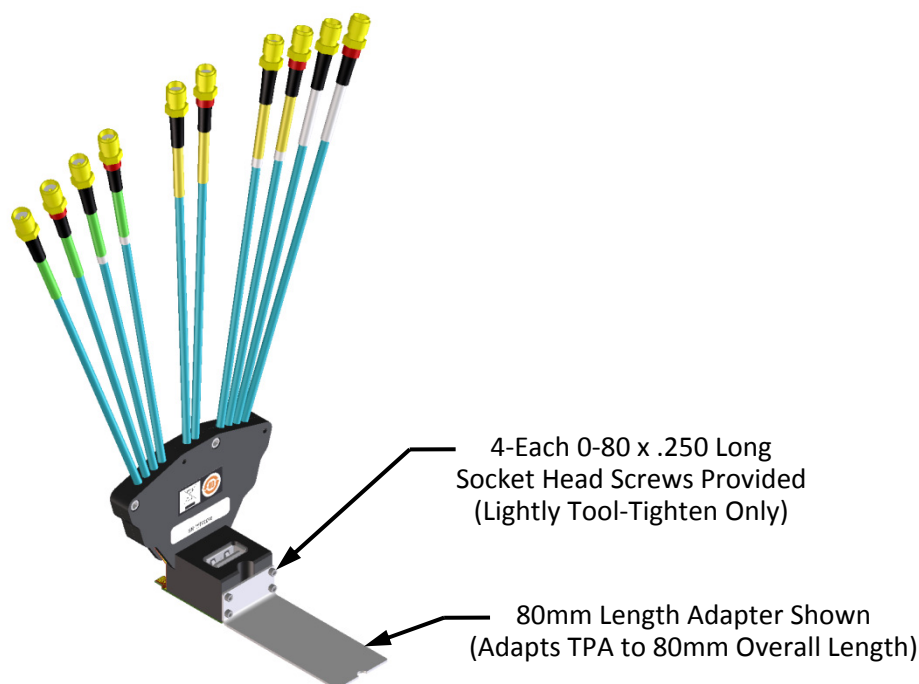
## PCIeM2-TPA2-P Optional Accessories

The PCIeM2-TPA2-P (Host TPA) can be optionally supplied with Host TPA Length Adapter materials. These materials allow the user to properly retain and stabilize the PCIe M.2 Host TPA when installed in host systems that are designed to accept devices with overall lengths of 42mm, 60mm, 80mm, or 110mm. The table below indicates the Wilder Technologies part numbers for an optional complete kit of length adapters and part numbers for individual specific-length adapters. The PCIeM2-TPA2-P (Host TPA) is 30 mm long without the optional Length Adapters.

**Table 11. Optional PCIe/SATA M.2 Host TPA Length Adapters**

| WILDER TECHNOLOGIES<br>PART NUMBER | DESCRIPTION                                                                |
|------------------------------------|----------------------------------------------------------------------------|
| 600-1096-000                       | Complete Kit – Contains Adapters for 42mm, 60mm, 80mm, 110mm, and Hardware |
| 600-1096-042                       | Contains Adapter for 42mm Applications and Mounting Hardware               |
| 600-1096-060                       | Contains Adapter for 60mm Applications and Mounting Hardware               |
| 600-1096-080                       | Contains Adapter for 80mm Applications and Mounting Hardware               |
| 600-1096-110                       | Contains Adapter for 110mm Applications and Mounting Hardware              |

The figure, below, illustrates the installation and typical application of the optional Host TPA Length Adapter materials.



**Figure 16. PCIeM2-TPA2-P Device Length Adapter**

## Wilder Technologies, LLC – Limited Warranty

Wilder Technologies, LLC warrants that each Test Adapter, 1) is free from defects in materials and workmanship and, 2) conforms to Wilder Technologies specifications for a period of 12 months. **See Consumable and Fragile Material Warranty for exceptions to the 12 month warranty**

The warranty period for a Test Adapter is a specified, fixed period commencing on the date of ship from Wilder Technologies, LLC. If you did not purchase your Test Adapter directly from Wilder Technologies, LLC, the serial number and a valid proof of purchase will be required to establish your purchase date. If you do not have a valid proof of purchase, the warranty period will be measured from the date of ship from Wilder Technologies, LLC.

If, during the warranty period, the Test Adapter is not in good working order, Wilder Technologies, LLC will, at its option, repair or replace it at no additional charge, except as is set forth below. In some cases, the replacement Test Adapter may not be new and may have been previously installed. Regardless of the Test Adapter's production status, Wilder Technologies, LLC appropriate warranty terms apply.

### **Consumable and Fragile Material Warranty**

Wilder Technologies, LLC warrants that consumable materials and all fragile materials supplied by Wilder Technologies, LLC either as part of an instrument or system, or supplied separately, will be free from defects in material and workmanship at the time of shipment.

### **Extent of Warranty**

The warranty does not cover the repair or exchange of a Test Adapter resulting from misuse, accident, modification, unsuitable physical or operating environment, improper maintenance by you, or failure caused by a product for which Wilder Technologies, LLC is not responsible. The warranty is voided by removal or alteration of Test Adapter or parts identification labels. The initial three months are unconditional; the remaining months excludes plugs, receptacles and SMA connectors. Connectors are wear items and excluded from the warranty after the initial three months.

**These warranties are your exclusive warranties and replace all other warranties or conditions, express or implied, including but not limited to, the implied warranties or conditions or merchantability and fitness for a particular purpose. These warranties give you specific legal rights and you may also have other rights which vary from jurisdiction to jurisdiction. Some jurisdictions do not allow the exclusion or limitation of express or implied warranties, so the above exclusion or limitation may not apply to you. In that event, such warranties are limited in duration to the warranty period. No warranties apply after that period.**

### **Items Not Covered by Warranty**

Wilder Technologies, LLC does not warrant uninterrupted or error-free operation of a Test Adapter.

Any technical or other support provided for a Test Adapter under warranty, such as assistance via telephone with "how-to" questions and those regarding Test Adapter set-up and installation, will be provided **WITHOUT WARRANTIES OF ANY KIND**.

### **Warranty Service**

Warranty service may be obtained from Wilder Technologies, LLC by returning a Wilder Technologies, LLC Returns Material Authorization and the Test Adapter to Wilder Technologies, LLC during the warranty period. To obtain RMA number, contact [support@wilder-tech.com](mailto:support@wilder-tech.com).

You may be required to present proof of purchase or other similar proof of warranty entitlement. You are responsible for any associated transportation charges, duties and insurance between you and Wilder Technologies, LLC. In all instances, you must ship Test Adapters in Wilder Technologies, LLC approved packaging. Information on packaging guidelines can be found at: [www.wilder-tech.com](http://www.wilder-tech.com). Wilder Technologies, LLC will ship repaired or replacement Test Adapter Delivery Duty Prepaid (DDP) and will pay for return shipment. You will receive title to the repaired or replacement Test Adapter and you will be the importer of record.

## Wilder Technologies, LLC – Terms & Conditions of Sale

1. **Other Documents:** This Agreement may NOT be altered, supplemented, or amended by the use of any other document(s) unless otherwise agreed to in a written agreement signed by both you and Wilder Technologies, LLC. If you do not receive an invoice or acknowledgement in the mail, via e-mail, or with your Product, information about your purchase may be obtained at [support@wilder-tech.com](mailto:support@wilder-tech.com) or by contacting your sales representative.
2. **Payment Terms, Orders, Quotes, Interest:** Terms of payment are within Wilder Technologies, LLC's sole discretion, and unless otherwise agreed to by Wilder Technologies, LLC, payment must be received by Wilder Technologies, LLC prior to Wilder Technologies, LLC's acceptance of an order. Payment for the products will be made by credit card, wire transfer, or some other prearranged payment method unless credit terms have been agreed to by Wilder Technologies, LLC. Invoices are due and payable within the time period noted on your invoice, measured from the date of the invoice. Wilder Technologies, LLC may invoice parts of an order separately. Your order is subject to cancellation by Wilder Technologies, LLC, in Wilder Technologies, LLC's sole discretion. Unless you and Wilder Technologies, LLC have agreed to a different discount, Wilder Technologies, LLC's standard pricing policy for Wilder Technologies, LLC-branded systems, which includes hardware, software and services in one discounted price, allocates the discount off list price applicable to the service portion of the system to be equal to the overall calculated percentage discount off list price on the entire system. Wilder Technologies, LLC is not responsible for pricing, typographical, or other errors in any offer by Wilder Technologies, LLC and reserves the right to cancel any orders resulting from such errors.
3. **Shipping Charges; Taxes; Title; Risk of Loss:** Shipping, handling, duties and tariffs are additional unless otherwise expressly indicated at the time of sale. Title to products passes from Wilder Technologies, LLC to Customer on shipment from Wilder Technologies, LLC's facility. Loss or damage that occurs during shipping by a carrier selected by Wilder Technologies, LLC is Wilder Technologies, LLC's responsibility. Loss or damage that occurs during shipping by a carrier selected by you is your responsibility. You must notify Wilder Technologies, LLC within 7 days of the date of your invoice or acknowledgement if you believe any part of your purchase is missing, wrong or damaged. Unless you provide Wilder Technologies, LLC with a valid and correct tax exemption certificate applicable to your purchase of Product and the Product ship-to location, you are responsible for sales and other taxes associated with the order. **Shipping dates are estimates only.**
4. **WARRANTY:** WILDER TECHNOLOGIES, LLC, warrants that the item(s) manufactured under the Buyer's contract shall be free from defects in materials and workmanship furnished by WILDER TECHNOLOGIES, LLC, and shall conform to the applicable drawings and specifications. WILDER TECHNOLOGIES, LLC'S liability herein, for breach of warranty, contract or negligence in manufacturing, shall be limited to repair or replacement. Repair or replacement of defective items will be applicable only if the Buyer notifies WILDER TECHNOLOGIES, LLC, by written notice within 30-days of delivery. All claims shall be addressed to: [support@wilder-tech.com](mailto:support@wilder-tech.com) or WILDER TECHNOLOGIES, LLC, 6101A East 18th Street, Vancouver, Washington 98661 U.S.A.; ATTENTION: Customer Service Manager. WILDER TECHNOLOGIES, LLC, reserves the right to inspect at the Buyer's plant all items claimed to be defective or nonconforming prior to authorizing their return. WILDER TECHNOLOGIES, LLC, assumes no liability for the results of the use of its components in conjunction with other electric, electronic or mechanical components, circuits and/or systems. The foregoing constitutes the sole and exclusive remedy of the Buyer and the exclusive liability of WILDER TECHNOLOGIES, LLC, and is IN LIEU OF ANY AND ALL OTHER WARRANTIES, STATUTORY, IMPLIED OR EXPRESSED AS TO MERCHANTABILITY, FITNESS FOR THE PURPOSE SOLD, DESCRIPTION, QUALITY, and PRODUCTIVENESS OR ANY OTHER MATTER. Without limiting the foregoing, in no event shall WILDER TECHNOLOGIES, LLC, be liable for loss of use, profit or other collateral, or for special and/or consequential damages.
5. **RETURNED GOODS:** WILDER TECHNOLOGIES, LLC, will accept only those goods for return that have been authorized for return. All goods authorized for return shall be assigned a Returned Material Authorization (RMA) Number. The RMA Number shall be clearly marked on the shipping container(s) and all documentation accompanying the goods authorized for return. The RMA Number shall be assigned by WILDER TECHNOLOGIES, LLC pursuant to the conditions set forth in Paragraph 4, WARRANTY.
6. **UNITED STATES GOVERNMENT CONTRACTS:** In the event this offer is accepted under Government contract, WILDER TECHNOLOGIES, LLC, agrees to accept clauses required by Government regulations and to waive WILDER TECHNOLOGIES, LLC conditions inconsistent therewith. WILDER TECHNOLOGIES, LLC, certifies that it is a regular manufacturer or dealer of the goods and/or services offered herein and that the prices offered do not exceed those charged to any customer for like quantities, services or materials under the same conditions.

## Compliance with Environmental Legislation

Wilder Technologies, LLC, is dedicated to complying with the requirements of all applicable environmental legislation and regulations, including appropriate recycling and/or disposal of our products.



### WEEE Compliance Statement

The European Union adopted Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE), with requirements that went into effect August 13, 2005. WEEE is intended to reduce the disposal of waste from electrical and electronic equipment by establishing guidelines for prevention, reuse, recycling and recovery.

Wilder Technologies has practices and processes in place to conform to the requirements in this important Directive.

In support of our environmental goals, effective January 1<sup>st</sup>, 2009 Wilder Technologies, LLC has partnered with EG Metals Inc. – Metal and Electronics Recycling of Hillsboro, Oregon, [www.egmetalrecycling.com](http://www.egmetalrecycling.com), to recycle our obsolete and electronic waste in accordance with the European Union Directive 2002/96/EC on waste electrical and electronic equipment ("WEEE Directive").

As a service to our customers, Wilder Technologies is also available for managing the proper recycling and/or disposal of all Wilder Technologies products that have reached the end of their useful life. For further information and return instructions, contact [support@wilder-tech.com](mailto:support@wilder-tech.com).

## Glossary of Terms

| TERMINOLOGY                | DEFINITION                                                                                                                                                                                                                            |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Aggressor                  | A signal imposed on a system (i.e., cable assembly) to measure response on other signal carriers.                                                                                                                                     |
| Decibel (dB)               | Ten times the common logarithm (i.e. log10) of the ratio of relative powers.                                                                                                                                                          |
| Informative                | The designation of a test that is not required for compliance but is considered important from a characterization standpoint. It is provided for informational purposes only.                                                         |
| Insertion loss             | The ratio, expressed in dB, of incident power to delivered power.                                                                                                                                                                     |
| PCIe                       | Peripheral Component Interconnect Express                                                                                                                                                                                             |
| PCIeM2-TPA2                | PCIe M.2 Socket 2 Test Point Access. A specialized assembly that interfaces to an PCIe M.2 Socket 2 receptacle or plug and enables access of signals for measurement or stimulation.                                                  |
| M.2                        | Formally called Next Generation Form Factor (NGFF)                                                                                                                                                                                    |
| Near-end crosstalk         | Crosstalk that is propagated in a disturbed channel in the opposite direction as the propagation of a signal in the aggressor channel. The terminals of the aggressor channel and the victim channel are usually close to each other. |
| Normative                  | The designation of a test that is required for compliance.                                                                                                                                                                            |
| Return Loss                | The ratio, expressed in dB, of incident power to reflected power.                                                                                                                                                                     |
| RoHS                       | Restriction of Hazardous Substances Directive                                                                                                                                                                                         |
| Serial ATA (SATA)          | Serial Advanced Technology Attachment or Serial ATA. The protocol defined by SATA (see ATA8-AAM)                                                                                                                                      |
| Serial Attached SCSI (SAS) | The set of protocols defined in SPL and the interconnect defined by the SAS-2.1 standard.                                                                                                                                             |
| USB                        | Universal Serial Bus                                                                                                                                                                                                                  |
| Victim                     | A signal carrier on a system that has a response imposed on it by other signals in the system.                                                                                                                                        |

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