PCIe Gen5 M.2 Test Adapters

Performance Report

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High-Speed Serial Results

The high-speed serial measurements of the PCIe Gen5 M.2 adapters use a 4-port (50-ohm) VNA calibrated from 50MHz to 40GHz with 800 points. The measurements are in the form of s-parameters.

The s-parameter measurements are renormalized to 42.5-ohm ports instead of 50-ohm ports. This was done so that the port impedance and adapter impedance match.

In addition, 2.92mm to MMPX adapters and MMPX connectors are included in the s-parameter measurements, but they are then gated out of the return loss due to their 50-ohm impedance.

Ultimately, this post-processing makes the s-parameters accurately represent the performance of the high-speed channels of only the M.2 adapters.

Characterization (CLB and CBB Independent Only):

To characterize the real high-speed channels of the adapters only (no connector), the replica channels must be used. These replica channels include MMPX connector lead-in for what would be the M.2 connector side of the high-speed channels. This MMPX connector lead-in that is part of the S-parameter measurement must then be de-embedded to represent the real high-speed channels.

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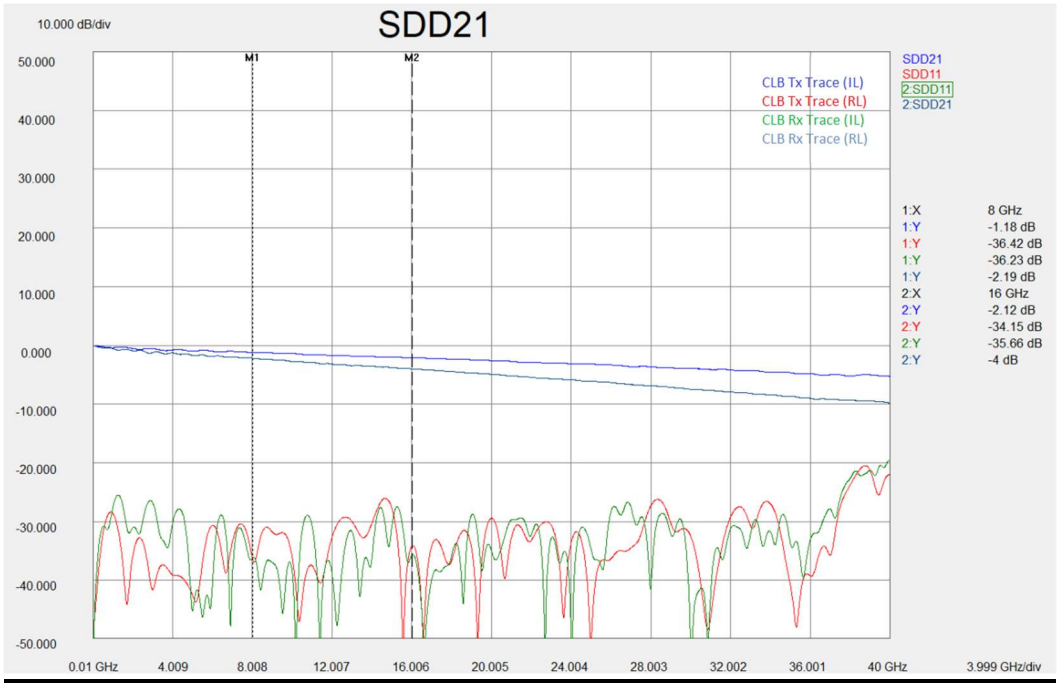
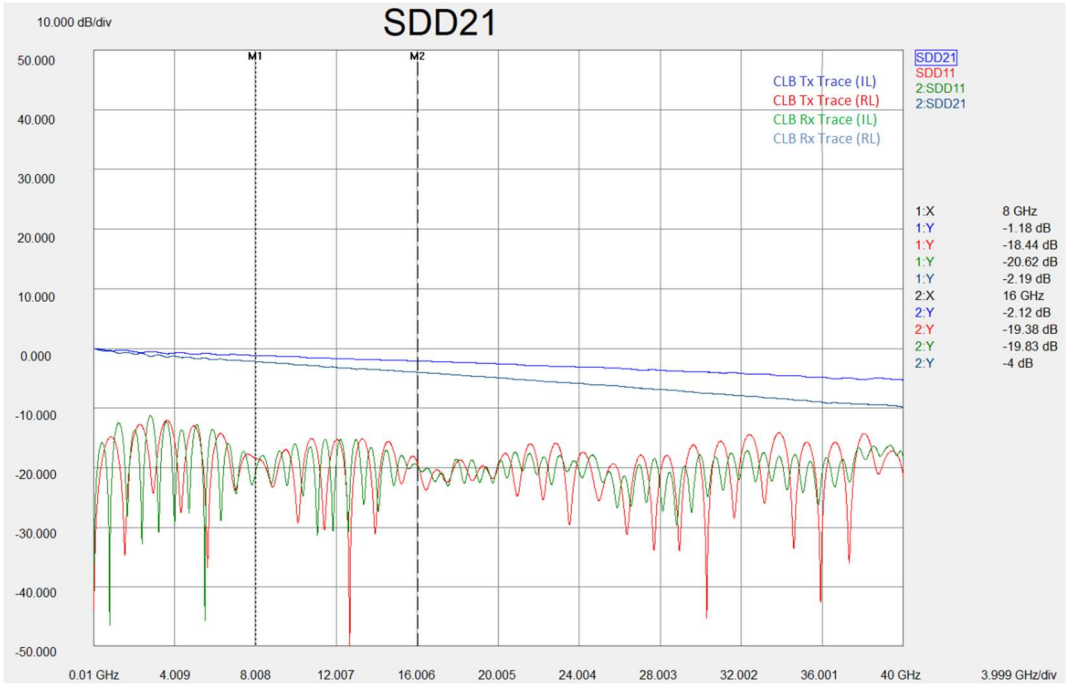
Figure 1: CLB Only Characterization



Corrected return loss maintains below 20dB.

Figure 2: CLB Only Characterization, No Correction or Gating



Uncorrected return loss maintains below 10dB.

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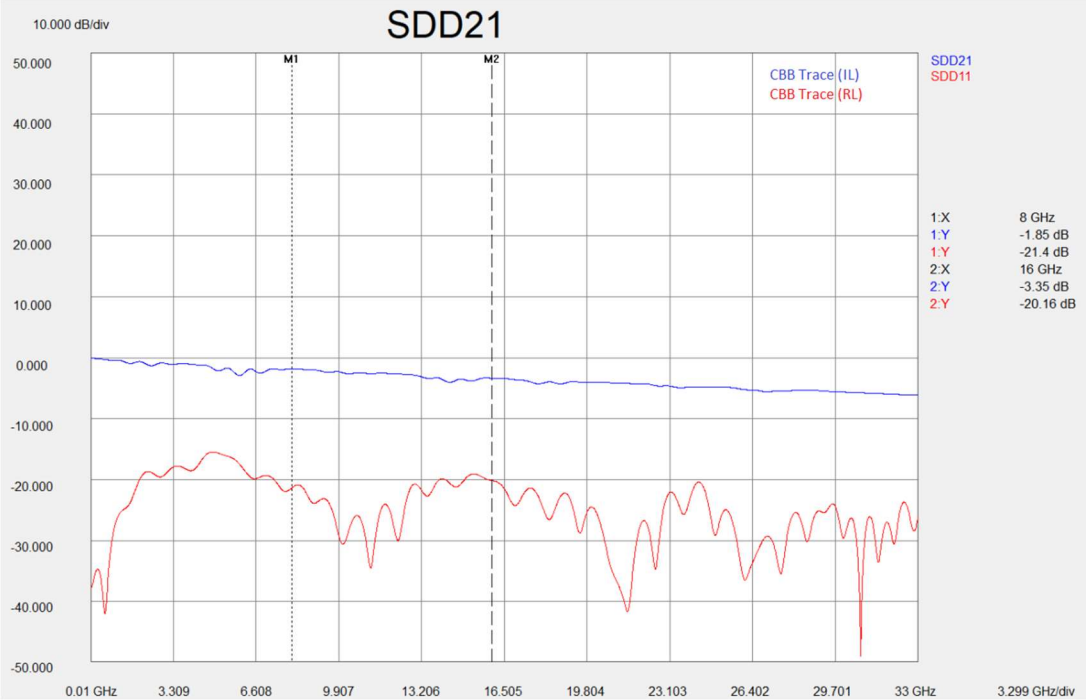
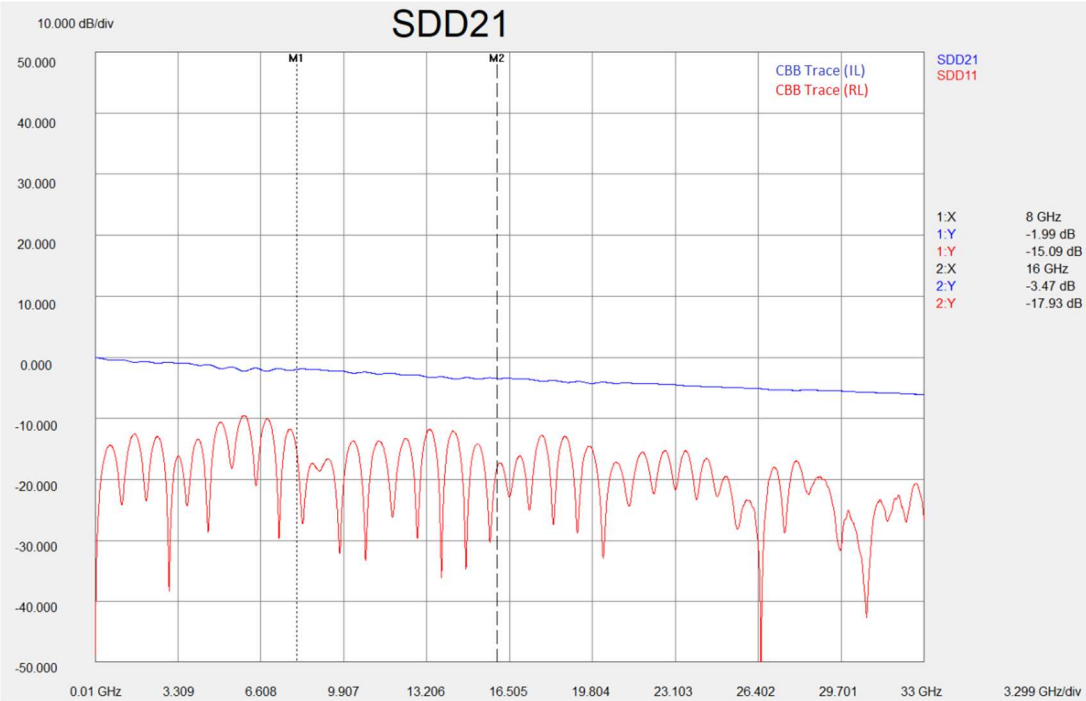
Figure 3: CBB Only Characterization



Corrected return loss maintains below 15dB.

Figure 4: CBB Only Characterization, No Correction or Gating



Corrected return loss maintains below 10dB.

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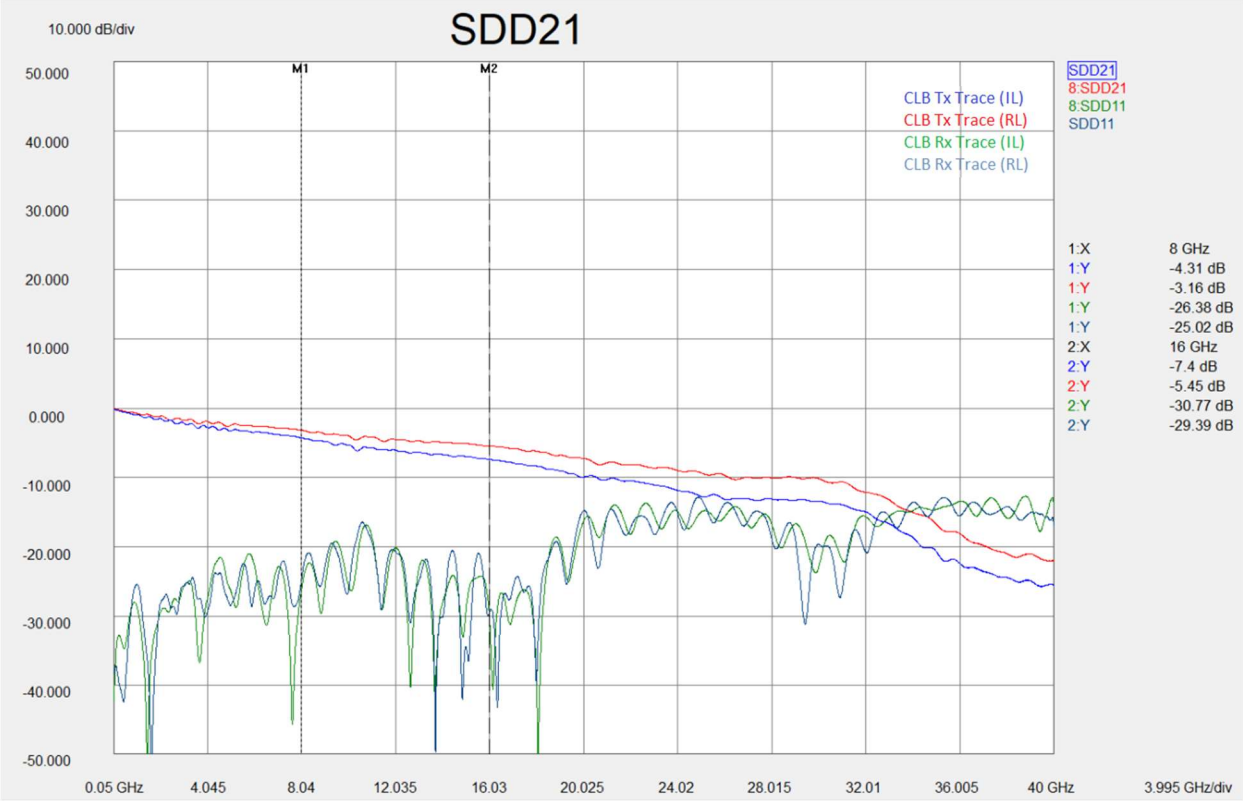
Mated CLB/CBB (CLB and CBB Independent Only):

These s-parameter measurements are made when the CLB and CBB are mated. The M.2 connector is included in the measurement. The MMPX connectors and 2.92mm to MMPX adapters are included in the s-parameter, but then are gated out.

Figure 5: CLB and CBB Mated Insertion and Return Loss



Return Loss is near or below -10dB from 10MHz to 40GHz. There are no significant resonances.

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Figure 6: CLB and CBB Mated Insertion and Return Loss, No Correction or Gating

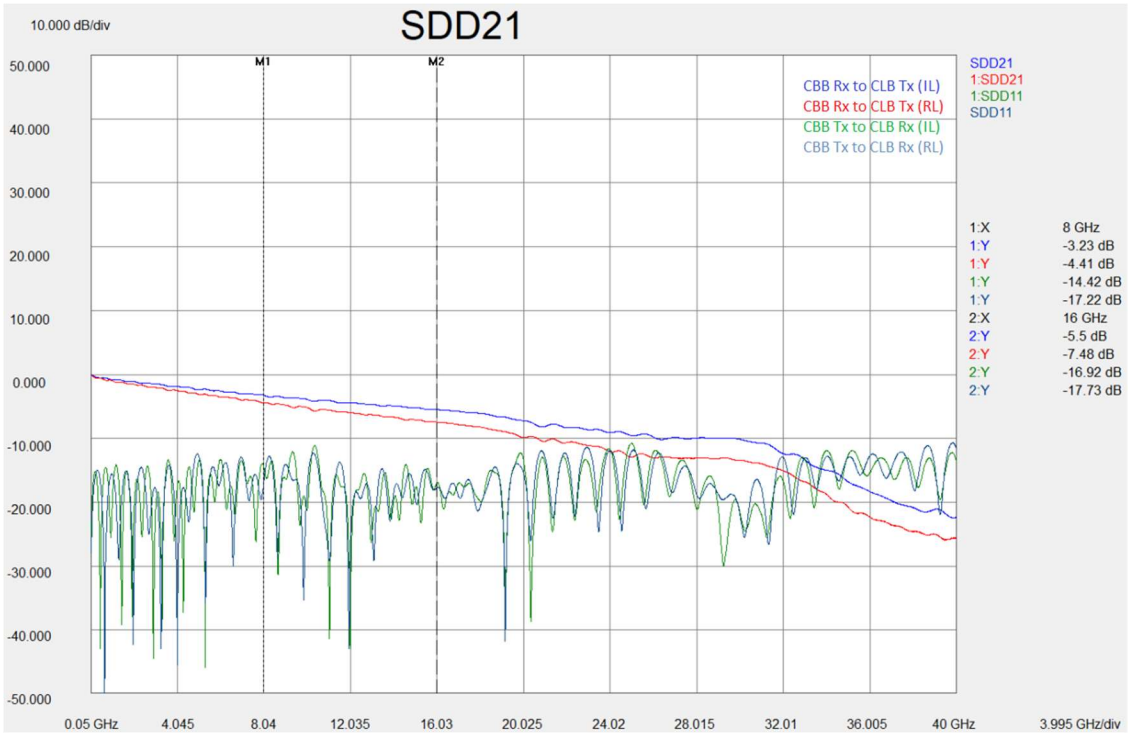
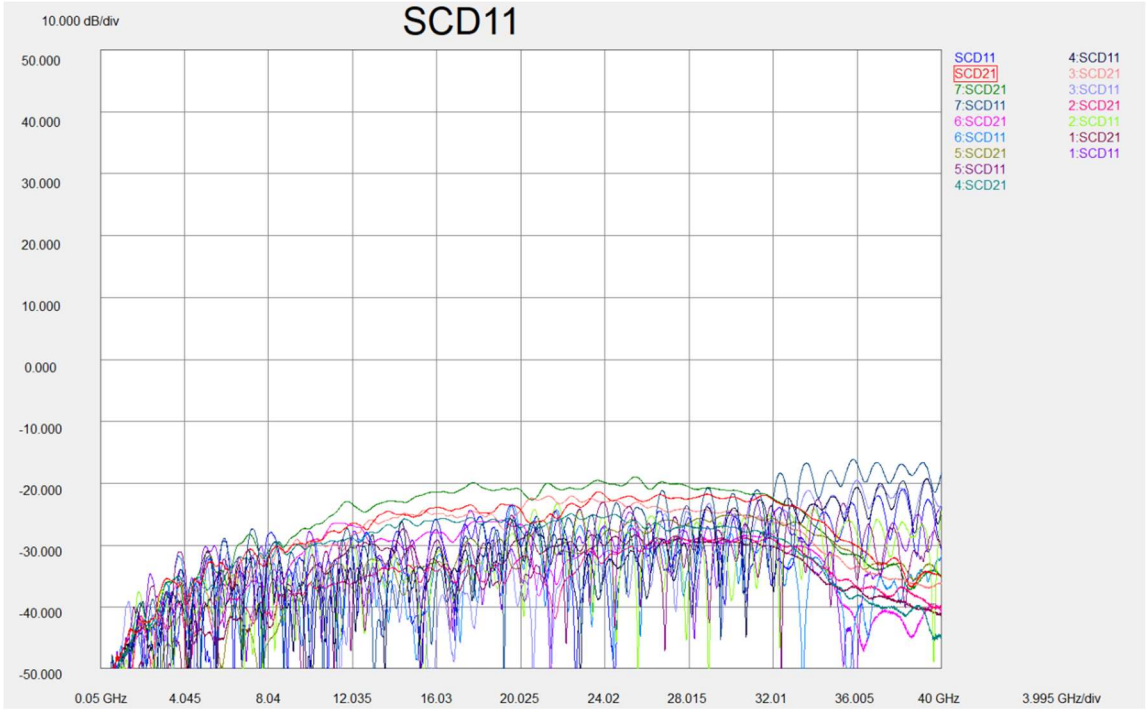


Figure 7: CLB and CBB Mated Conversion Loss



Maintains below -20dB for all frequencies except after 32GHz.

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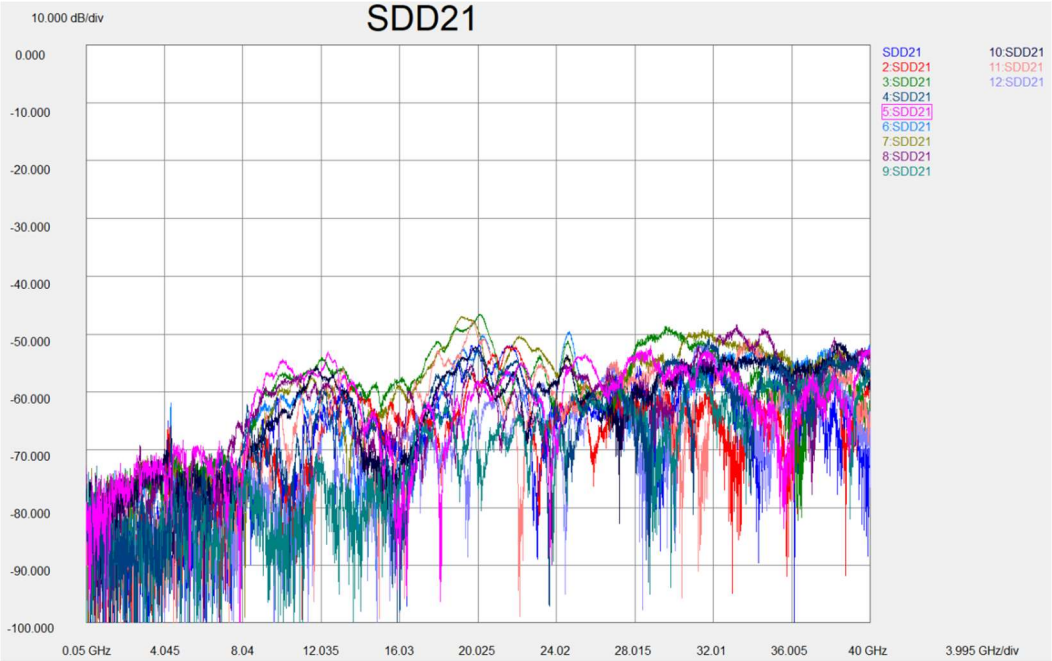
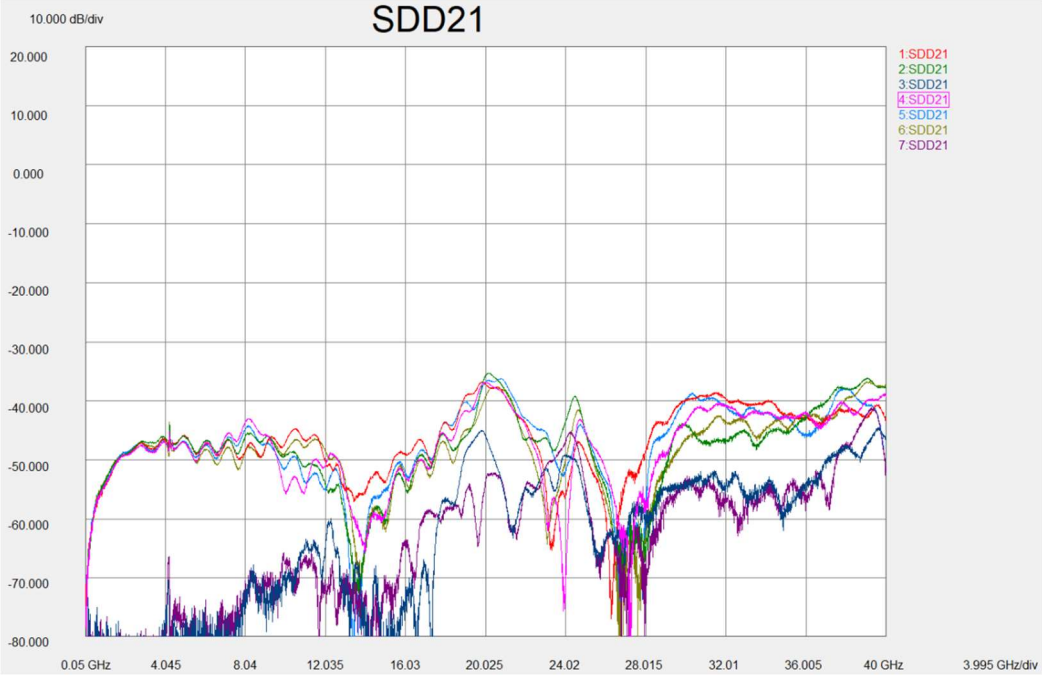
Figure 8: CLB and CBB Mated FEXT



Maintains at or below -44dB for all frequencies.

Figure 9: CLB and CBB Mated NEXT



Maintains at or below -35dB for all frequencies.

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Fixture Test Channel Setup:

Figure 10: Total Test Channel Loss for Gen5

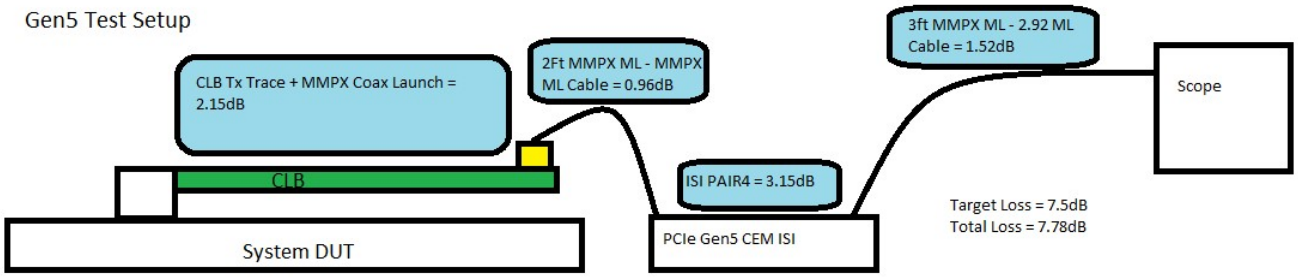
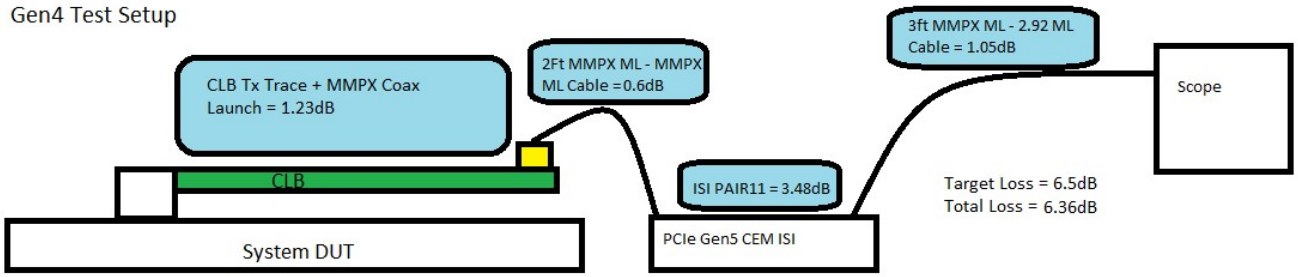


Figure 11: Total Test Channel Loss for Gen4



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Voltage Rail Results

Loading:

An electronic load is connected to each voltage rail one at a time with the load according to the peak current values in the figure from the M.2 specification shown below.

Figure 12: Table 4-23 from PCI Express M.2 Specification

Table 4-23. Power Rating Table for M.2 Add-in Cards

Key	Power Rail	Voltage Tolerance	Current Consumption Limit	
			Peak (Note 1) mA Max Avg @ 100 µs	Normal (Note 2) mA Max Avg @ 1 s
A	3.3 V	± 5%	2000	
B	3.3 V	± 5%	5000 (Note 6)	2500 (Note 5)
B	V_{BAT} (Note 3)	3.135 V to 4.4 V	2500	
C	3.3 V	± 5%	2500	
C	V_{BAT}	3.135 V to 4.4 V	2500	
C	VIO 1.8 V	± 5.55% (Note 4)	70	
D	RFU	RFU	RFU	RFU
E	3.3 V	± 5%	2000	
F	RFU	RFU	RFU	RFU
G	N/A	N/A	N/A	N/A
H	RFU	RFU	RFU	RFU
J	RFU	RFU	RFU	RFU
K	RFU	RFU	RFU	RFU
L	RFU	RFU	RFU	RFU
M	3.3 V	± 5%	7000 (Note 6)	3500 (Note 5)
M	VIO 1.8 V	± 5.55% (Note 4)	70	

Notes:

1. Peak is the maximum highest averaged current value over any 100 µs period
2. Normal is the maximum highest averaged current value over any 1 s period
3. Power Rail connection alternative for WWAN specific Adapters only. Not supported by other Socket 2 Adapter types such as SSDs
4. 1.7 V to 1.9 V Range
5. Normal currents assume sufficient power dissipation capability by the Platform. This capability is outside the scope of this specification. The maximum power of device may be controlled through function specific capabilities (e.g., for SSDs see NVMe).
6. The peak current's duty cycle shall ensure that the normal current is not violated.

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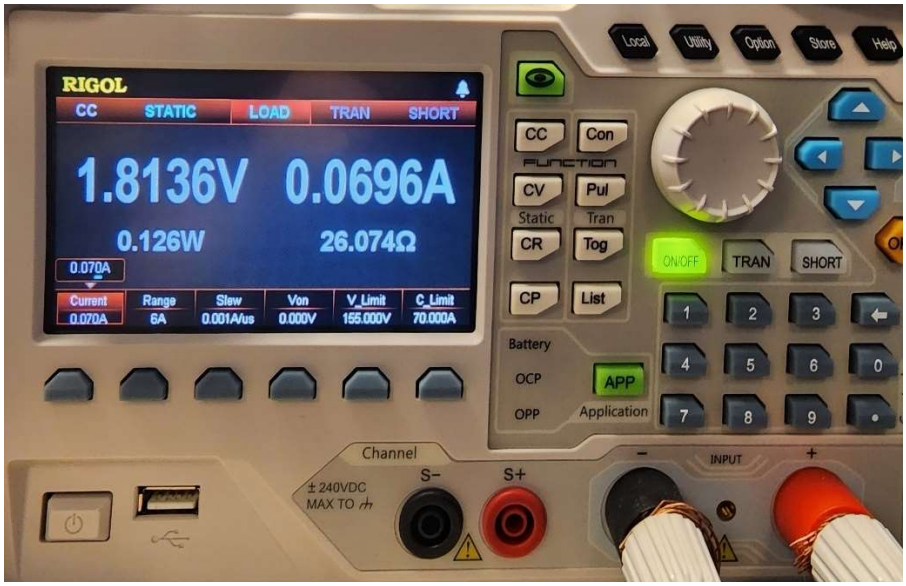
Figure 13: Electronic Load Results for the 3.3V Rail

Figure 14: Electronic Load Results for the 1.8V Rail



The voltage is within the tolerance at the CBB test points. The voltage rails are successfully loaded with no unexpected voltage drops and no overheating.

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Sequencing:

In this section, the 1.8V rail start-up time is compared against the 3.3V start-up time.

This comparison is accomplished using an oscilloscope with header connection probes. They connect at the test points near the voltage converters.

Figure 15: Voltage Rail Sequence Test Measurement

Sequence Delay (1.8V Rail) = 9.711ms

M.2 states that the 3.3V rail needs to meet at least 300mv before the 1.8v rail is switched on. Additionally, the 3.3v rail needs to remain at least 200mv higher than the 1.8V rail. The 3.3V rail fully powers for about 10ms before the 1.8V rail powers on meeting the power on requirements.

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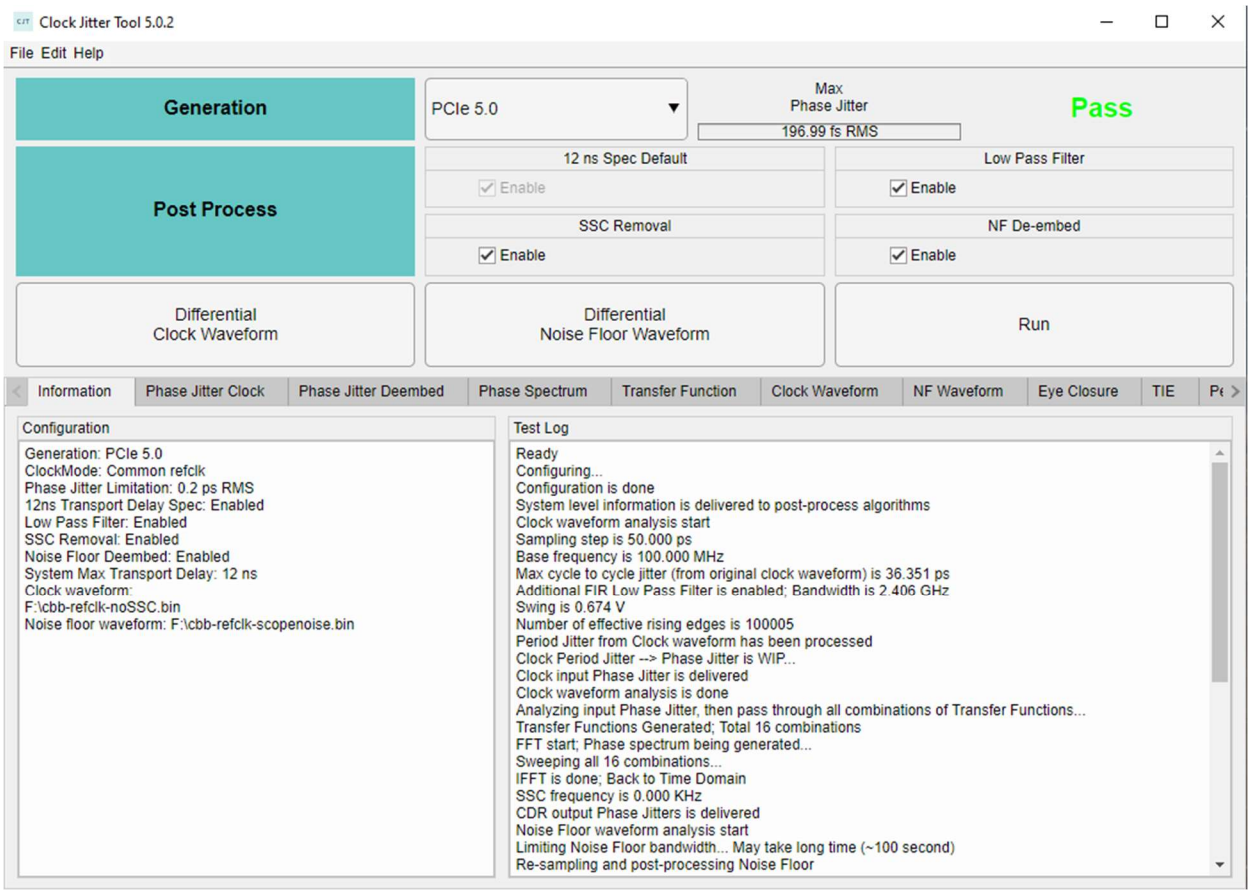
REFCLK Results (CBB Independent Only)

A differential probe along with 2.92mm to MMPX cables were used to measure the REFCLK waveform generated by the CBB independent adapter on the oscilloscope.
This waveform was then saved to a .bin file and imported into the Clock Jitter Tool.
PCI-SIG website provided a link to this test tool.

Jitter:
REKCLK passes phase jitter requirements.
The max phase jitter shows 196.99 fs RMS which is below 200fs RMS limit in the PCIe specification.
Note: Real Time Scope noise has been removed during post processing.

Figure 16: Clock Jitter Tool Results Window



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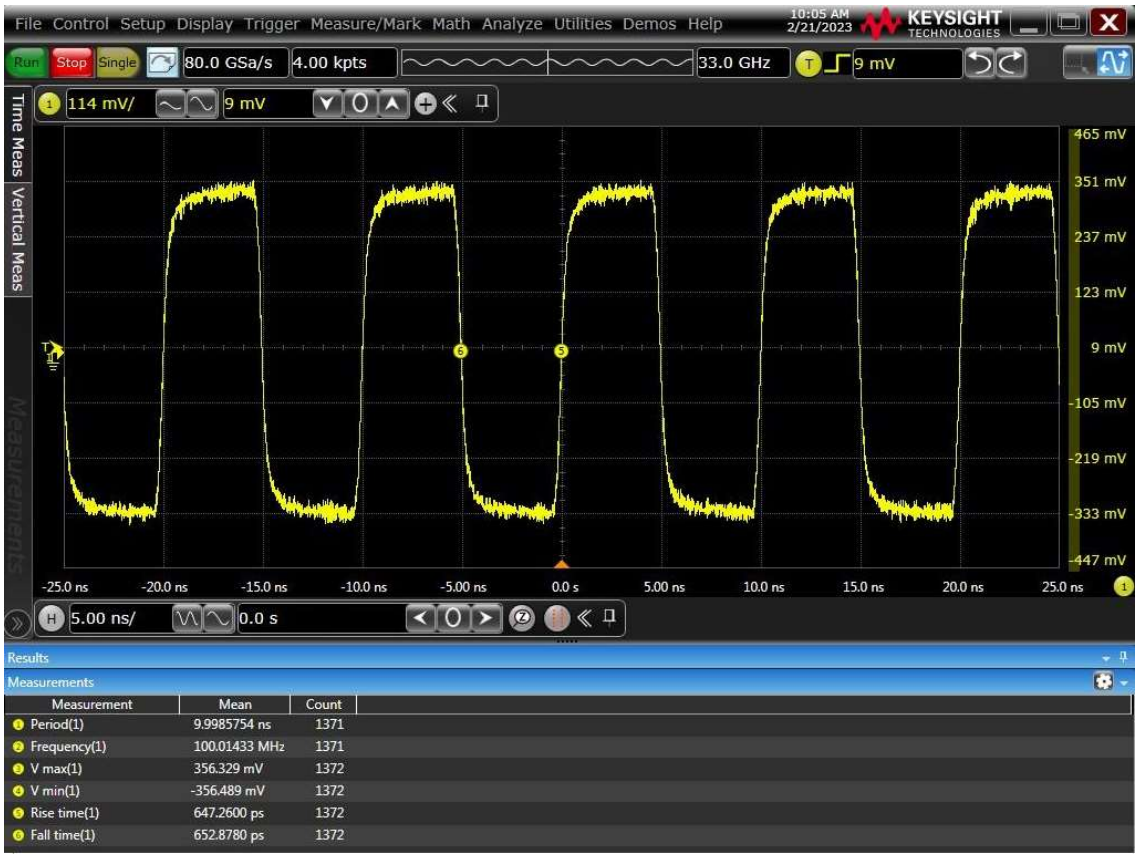
Characteristics:

Period: 9.9985754ns, Pass
V max/mind: +/-356mV, Pass
Rise time: 647ps, Rise Time Rate: 0.88V/ns, Pass
Fall time: 653ps, Fall Time Rate: 0.87V/ns, Pass

Figure 17: REFCLK Characteristics on Real Time Oscilloscope



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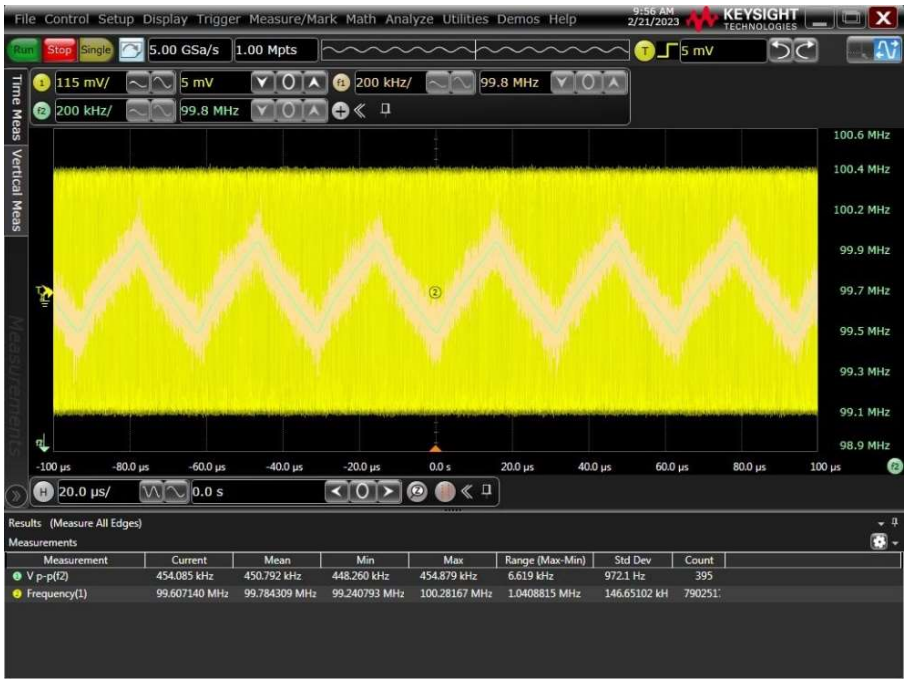
SSC:

Figure 18: REFCLK with SSC set at -0.5% down spreading



SSC Setting: -0.5%, Actual -0.45%

Figure 19: REFCLK with SSC set at -0.5% down spreading

SSC Setting: -0.25%, Actual -0.27%

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CMTS (Compliance Mode Toggle Signal) Results

A differential probe along with 2.92mm to MMPX cables were used to measure the CMTS waveform and equalization presets on the oscilloscope. CMTS push button was used to activate the CMTS.

Characteristics:

Figure 20: 40mV Noise Test of CMTS

The noise is under +/-40mV before and after the trigger of CMTS.

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Figure 21: CMTS Frequency

The CMTS frequency shows a mean of 99.989021MHz.

Figure 22: CMTS Pulse Length

The CMTS time length is 1ms.

These characteristics are adequate for toggling transmitter equalization presets.

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DUT Compliance toggling:

The CMTS signal successfully toggles compliance toggle patterns in an M.2 PCIe Gen 5 system and those measurements are shown below.

Figure 23: Measured Compliance Patterns on GEN5 System DUT (32GT/s PCIe 5.0 PRESET 0)

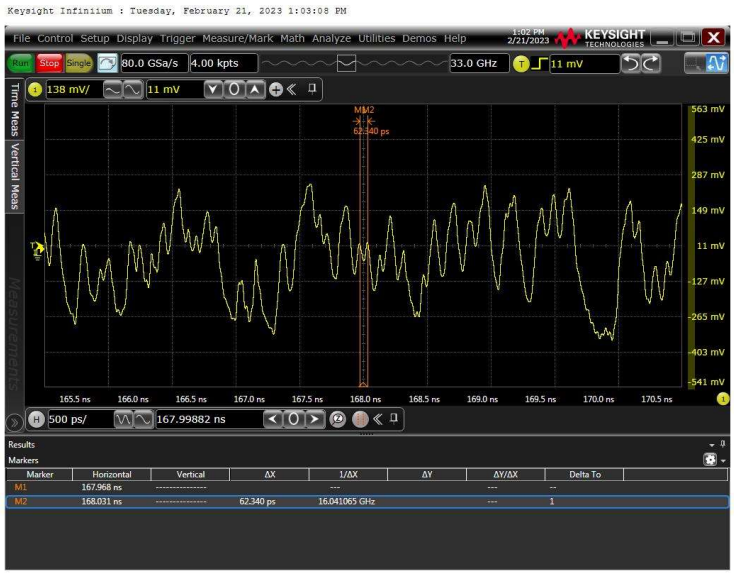

Figure 24: Measured Compliance Patterns on GEN3 AIC DUT (8.0GT/s PCIe 3.0 Preset 0)

The M.2 Test Adapters support PCI Express systems that use PCIe Gen 5. The test measurements for Gen5 AIC DUT are not shown in this report.

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PERST Results

This PERST test is accomplished using an oscilloscope with header connection probes. They connect at the 1.8V rail test point and the PERSTn trace on the CBB.

The voltage rail and PERSTn transition can be seen on the oscilloscope on CBB start-up. The PERSTn transition can also be seen when the PERST button is pressed on the CBB. The delay between these transitions is then measured on the oscilloscope.

Automatic (Start-Up):

Designed delay = 100ms

Measured delay = 103.58ms

The figure below shows the delay between the 1.8V rail and PERSTn signal.

Figure 25: Delay Measurement between 1.8V rail start-up and PERSTn Rise on Real-Time Oscilloscope

Manual (Push-Button Activated):

Designed delay = 100ms

Measured delay = 103.84ms

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The figure below shows the delay between PERST button push and PERSTn signal.

Figure 26: Delay Measurement After PERST Button Press on Real-Time Oscilloscope

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